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A HIGH SPEED SEQUENTIAL DECODER

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A HIGH SPEED SEQUENTIAL DECODER

By Henry Lum, Jr.

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SUMMARY

The performance and theory of operation for the High Speed Hard Decision Sequential Decoder are delineated in this report. The decoder is a forward error correction system which is capable of accepting data from binary-phase-shift-keyed and quadriphase-shift-keyed modems at input data rates up to 30 megabits per second. Test results show that the decoder is capable of maintaining a composite error rate of 1×10^{-5} at an input E_b/N_o of 5.6 dB. This performance has been obtained with minimum circuit complexity.

1. INTRODUCTION

The High Speed Hard Decision Sequential Decoder (HDSD) developed by Linkabit Corporation under Contract NAS2-6411 is a forward error correction system which is capable of accepting data from binary-phase-shift-keyed (PSK) and quadriphase-shift-keyed (QPSK) modems at data rates up to 30 megabits per second. The HDSD uses a constraint length k=41 or k=33, rate 1/2, systematic convolutional code which is transparent to 180° phase ambiguities. All synchronization circuits are contained within the HDSD and the system does not require frame or block synchronization.

The development of the HDSD followed a feasibility study contract (NAS2-6024) completed by Linkabit Corporation in January 1971. Investigations of coding systems which could be utilized for high data rate links were accomplished under this contract. High decoder performance with minimum circuit complexity was established as the contract goal. The HDSD development was undertaken to investigate the feasibility of constructing a hardware coding system with commercial logic elements, for operation at extremely high speeds.

The test results indicate that the performance goals established in the feasibility study contract have been achieved. The HDSD shows a performance gain of 4.0 dB (worst case E_b/N_0) over an uncoded system at an input data rate of 35 megabits per second (Mbps) and an output error rate of $1x10^{-5}$. The signal energy transmitted by an uncoded system would have to be more than doubled to achieve these same performance goals. The performance gain at lower data rates, e.g., 2 Mbps, is slightly greater, approximately 4.5 dB over an uncoded system.

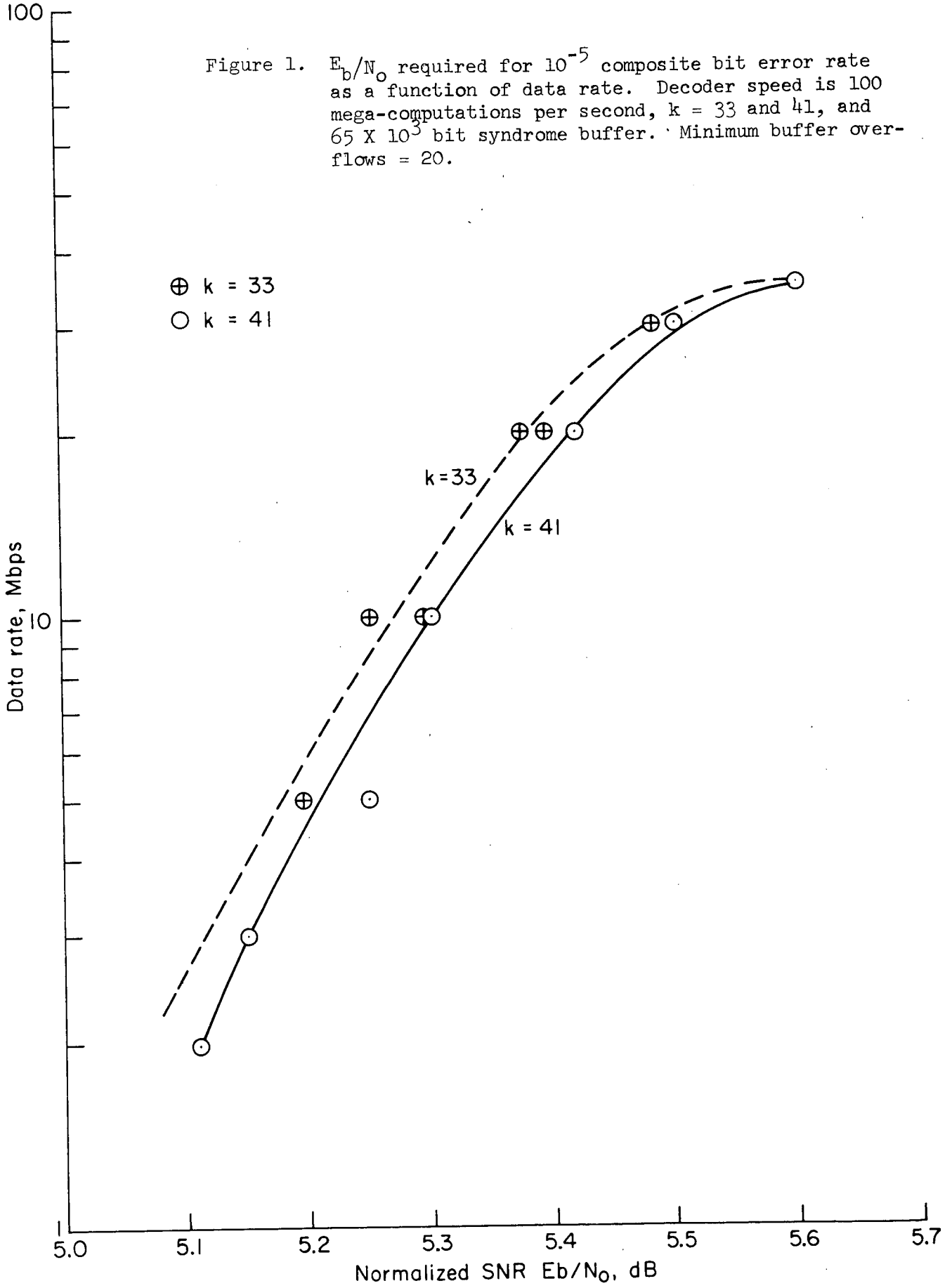
1.1 Test Results

The decoder was first evaluated in the operational mode which would achieve error rates as low as 10^{-8} with relatively little additional signal power. The configuration of the decoder was as follows: constraint length k=41, memory size of 65k bits, and a computation rate of 100 MHz. The composite output error rate was held constant at 10^{-5} and the input errors were varied at each of the selected data rates to achieve the specified composite output error rate. (The composite output error rate is the overall system error rate which includes errors caused by memory overflows as well as undetected errors.)

The performance of the decoder is shown in figure 1, wherein the input data rate (input symbol rate is twice the data rate) is plotted against the normalized signal-to-noise ratio (SNR $\triangleq$ E_b/N_0) of the input data bits. The performance curve exhibits the following characteristics for the Hard Decision Sequential Decoder (HDSD): At lower data rates, less signal energy is required to achieve a composite output error rate of 10^{-5}; as the data rate is increased, more signal energy is required to maintain the specified performance up to its asymptotic limit (approximately 35 megabits per second (Mbps) input data rate). The required signal energy is lower at the low data rates due to the increase in the speed factor, which is defined as the ratio of the computation rate to the data rate. (A computation is the evaluation and testing of a metric value as the HDSD "looks" forward or backward one branch of the state-diagram or trellis diagram.) The significance of the increased speed factor is that the HDSD is able to perform a greater number of computations for each bit decoded. As the data rate is increased, the average number of computations permitted per bit is decreased and hence, the signal energy must be increased to maintain the composite error rate of 10^{-5}.

The asymptotic limit of the HDSD is reached at the 35 Mbps data rate due to the accumulation of propagation delays for various signals throughout several circuit boards, especially in the Input/Output board. This performance limitation could be improved

Figure 1. E_b/N_o required for 10^{-5} composite bit error rate as a function of data rate. Decoder speed is 100 mega-computations per second, k = 33 and 41, and 65×10^3 bit syndrome buffer. Minimum buffer overflows = 20.



by the optimization of the signal paths in all the circuit boards but this would involve extensive test time and redesign, especially in the physical placement of circuit elements on the board.

If the constraint length k is changed from 41 to 33 with all other conditions maintained constant (computation rate at 100 MHz, composite error rate at 10^{-5}, and variable input errors), the performance of the HDSD is slightly improved as shown in figure 1. This improved performance is due to a shorter decode path (the number of possible decoding states in a state-diagram increases exponentially with the constraint length k) which results in a decreased number of overflows. (An overflow occurs when the number of branches of received data in the buffer waiting to be decoded exceeds the buffer size.) As the overflows decrease, undetected errors increase, (due to the less powerful coding performance with a shorter constraint length code) but are not as great as the errors due to overflows. Hence, the composite error rate is decreased, showing an improvement in the HDSD's performance at the specified evaluation parameters. However, if the signal input energy is decreased (E_b/N_0 is lower than 5.0 dB), the composite error rate curve for the HDSD will shift to the right of the k=41 curve, i.e., the HDSD performance with a constraint length k=41 will be better.

The difference in performance can be readily understood if one examines the HDSD system operation during an overflow condition. When overflows occur, they typically come in bursts of 17 or more. The burst condition is the effect of many resync trials which the HDSD must undergo before it can successfully start decoding again. During this time the data is completely uncorrected and many errors (typically 10 errors per overflow) occur. If the input SNR is maintained at a fairly reasonable level, e.g., approximately 5.2 dB, then the overflows can be reduced by a reduction in the constraint length, i.e., k=41 to k=33. This has the effect of a shorter decoding path; undetected errors will be higher for the k=33 length, but the number of undetected errors will still be lower than that resulting from an overflow condition. Hence, the composite error rate of the system will be improved.

The equipment performance will also be affected by changing two other variables, Memory Size and Computation Rate, which are controlled by front panel switches. Both parameters will decrease the performance capabilities of the HDSD. If for some reason the maximum coding delay cannot be tolerated, the memory size can be decreased; however, the system will not perform as effectively in the state-diagram search as with the maximum memory size. Here, performance will be traded for shorter decoding delays. Use of the 1 MHz computation rate is primarily for test purposes, i.e., signal tracing is much easier at a lower data and computation rate.

Operation of the HDSD at input data rates greater than 30 Mbps is not recommended. As the speed of the system is increased, additional heat is generated by the shift registers (saturated logic) which, in turn, causes an additional heat rise on the MECL 10,000 series. This additional heat rise may have been the contributing factor in the failure of several MECL 10,000 devices at the higher data rates.

1.2 Recommendations

The HDSD development was undertaken to determine the feasibility of data decoding at very high input data rates. However, if it is anticipated that the unit will be made part of an operating system, it is recommended that the following actions be undertaken to optimize the performance of the Hard Decision Sequential Decoder:

(a) Locate the "hot spots" in the equipment, measure the temperature rise of critical circuits, and redesign the board if necessary.

(b) Measure the propagation delay of all critical signals and redesign the circuit as required.

(c) Investigate new fabrication methods, e.g., stack-type construction similar to hybrid circuits using integrated circuits dies. This will greatly reduce the propagation delay.

(d) Conduct more extensive data tests to determine the influence of different parameters, e.g., constraint length, speed-up factor, etc., on the composite error rates at different input data rates.

2. GENERAL SYSTEM OPERATION

2.1 System Test Arrangement

The Hard Decision Sequential Decoder was evaluated with the NASA/Ames High Speed Data Test Set. The test configuration shown in figure 2 was used to evaluate the system. The High Speed Test Set contains a data generator (511 bit PN sequence and a fixed format sequence), data encoder, a digital noise generator, and a data multiplexer. The error counter, also designed and built by ARC, contains an overflow counter and a self-synchronizing error comparator. Information on the Digital Noise Generator is included in Appendix I of this report. The convolutional encoder is a rate 1/2 systematic coder with constraint lengths of k=33 and k=41. The shift register taps for the generation of the parity bits correspond to a connection vector of 71547370131746 (octal representation).

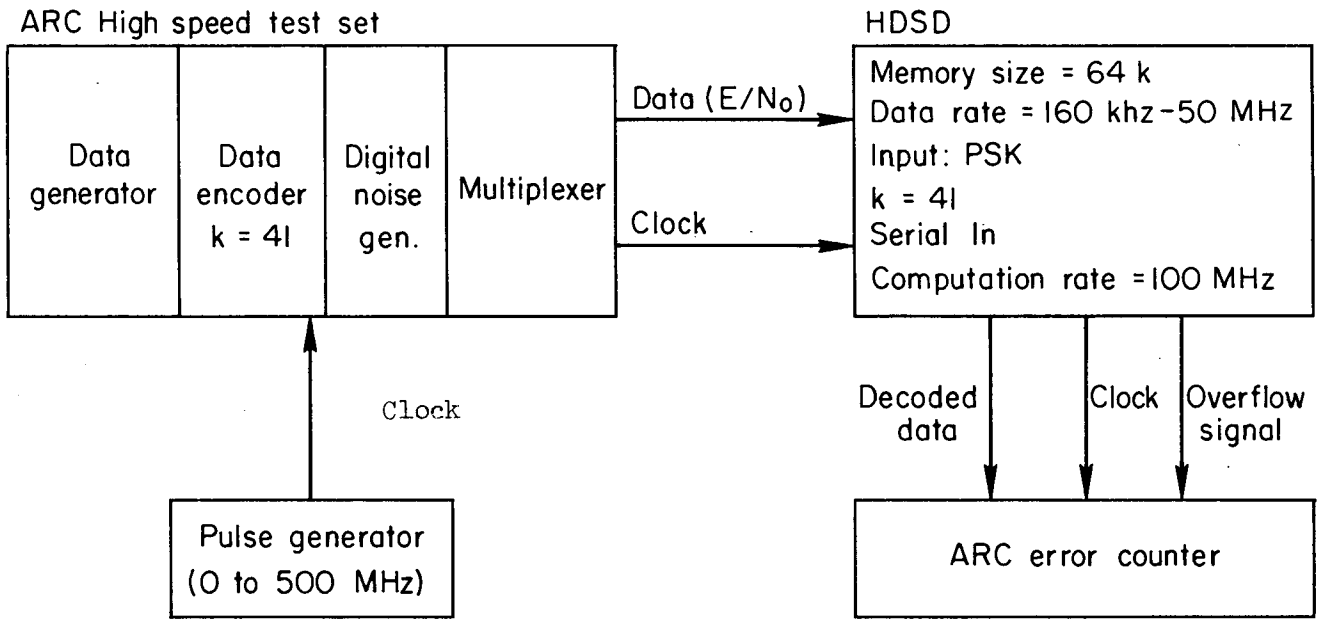


Figure 2. HDSD/ARC High speed data test set interface.

2.2 Description of the Hard Decision Sequential Decoder

All external controls for the HDSD are located on the front panel of the unit and are shown in figure 3. A description of each of the controls follows:

(a) On-Off Control

The on-off control is mounted on the left center of the front panel. It is a lighted, push-on, push-off type switch.

(b) Clear Switch

The clear switch is mounted in the right center of the front panel. It is a lighted push button momentary contact type switch. The function of the clear button is to reset the internal state of the decoder. It must be depressed when the unit is turned on and whenever the data rate range switch or the memory size is changed. The clear switch is also used to clear the decoder from a bad system state.

(c) Constraint Length Switch

The constraint length switch is a two position toggle switch. In one position, the decoder will decode data which was encoded by a constraint length 41 encoder. In the other position, the constraint length is 33.

(d) Memory Size Control

The memory size control is located in the upper left corner of the panel and is an eight position rotary switch. The function of the memory size switch is to control the total delay through the decoder. The delay through the decoder is variable from 1,000 bits to 64,000 bits. The minimum memory size in the highest data rate range is 4,000 bits. Normally, the largest memory size consistent with the tolerable decoding delay should be used, as this will result in the best performance. Whenever the position of the memory size switch is changed, the clear button must be depressed in order to enter the new position of the switch into the decoder.

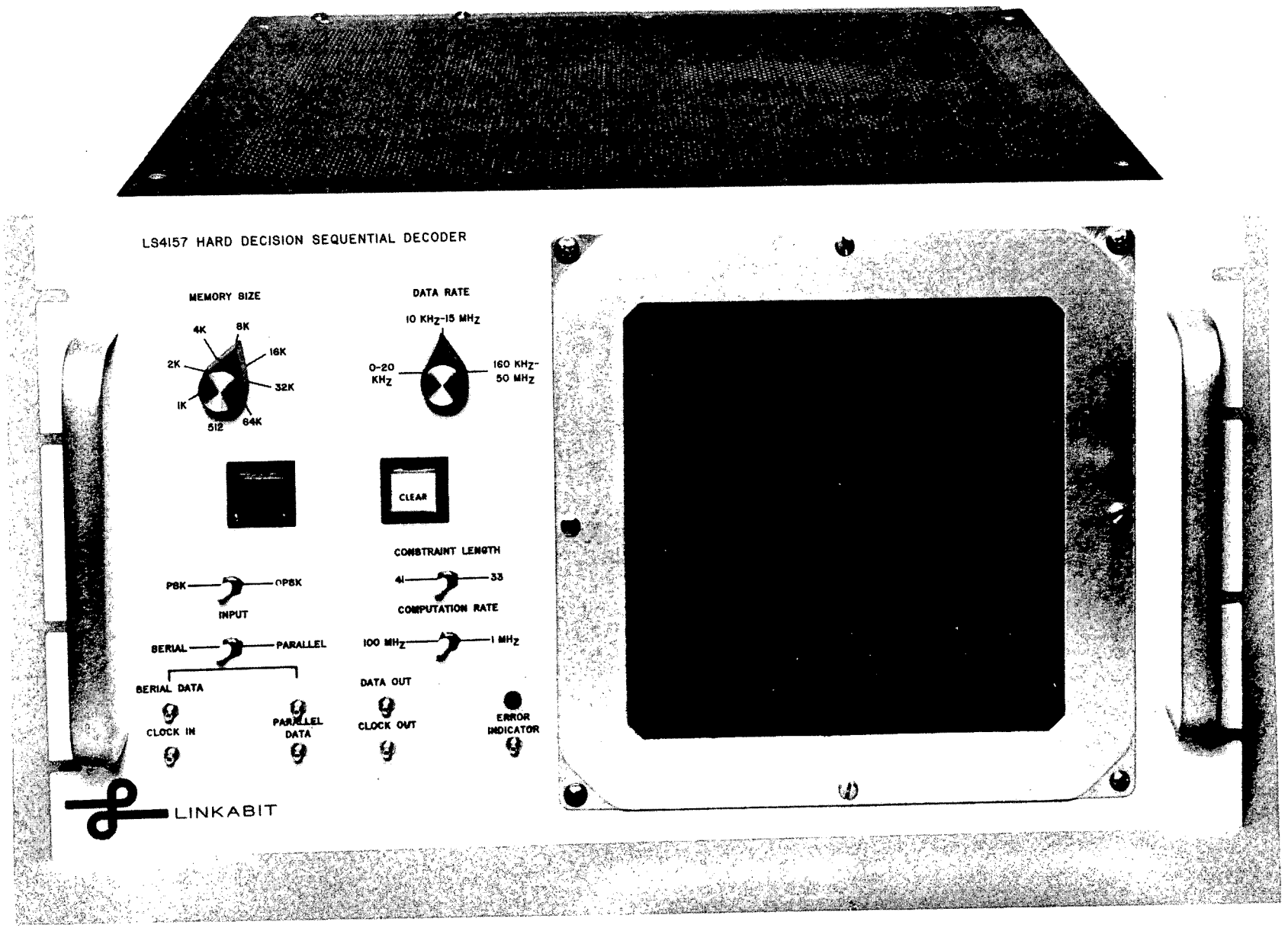


Figure 3. LS4157 Hard Decision Sequential Decoder

(e) Data Rate Range

The data rate switch is located in the upper right portion of the panel and is a three position rotary switch. Three overlapping data rate ranges are provided: 0 through 20 kHz, 10 kHz through 5 MHz, and 160 kHz through 50 MHz. The clear switch must be depressed after changing the data rate range.

(f) Serial/Parallel Control

The serial/parallel control is located in the lower left portion of the front panel and is a two position toggle switch. The switch controls the format of the input data. In the serial mode, data from the serial data input is clocked in at the symbol rate and converted to two line parallel data at the data rate. The input symbol rate clock is divided by two and provided as the output clock.

(g) PSK/QPSK Control

The PSK/QPSK Control is a two position toggle switch and is located in the lower left portion of the front panel. This control affects the operation of the node sync circuitry. In the PSK mode, when the node sync circuitry determines that the present node sync is incorrect, the node sync causes the timing to slip one symbol clock time. In the QPSK mode, when a bad node sync state is detected, the node sync is changed by interchanging two successive symbols and inverting one.

(h) Computation Rate Switch

The computation rate switch is located in the lower right portion of the panel and is a two position toggle switch. In one position, the internal computation rate of the decoder is at its maximum. In the other position, the internal computation rate of the decoder is divided by 128. The main use of this control is during system checkout. Normally it is desirable for the computation rate to be as high as possible since this results in the best performance.

(i) Error Indicator

The error indicator will light whenever the decoder determines that the output data is unreliable. There are three conditions that can cause the error indicator to light: depressing the clear switch, a node sync

state change, and a main memory buffer overflow. In the first two conditions, if the error indicator comes on, it will remain on until one buffer full of data is clocked out. In the case of buffer overflow, the indicator will stay on for 500 bit times or more, depending on the input error rate.

If the error indicator turns on and remains on, then either the input error rate is too high, the decoder inputs are improperly connected, or the decoder is malfunctioning.

2.3 Installation

2.3.1 General

The Hard Decision Sequential Decoder (LINKABIT LS4157 system) is packaged for standard 19-inch rack installation. However, the system can be operated in any configuration, the only requirement being that the fans be unimpeded and either the top or bottom -- preferably both -- be free to pass the exhaust air. A block diagram of a communication system utilizing the LS4157 is shown in figure 4. The decoder is located between the receiver modem and data sink.

2.3.2 Connection of Power Cable

The power cable from the decoder chassis must be connected to the two terminal blocks on the rear of the power supply chassis. The power cable contains switched AC power to the power supplies and power, sense, and ground wires. Connect the power cable to the power supply in accordance with figure 5 (drawing WD 1025). USE EXTREME CARE. If the cable is connected incorrectly, the system can be seriously damaged. The cable has been laced so that errors are difficult, however, the possibility of incorrect connection remains. It is, therefore, STRONGLY RECOMMENDED that all circuit boards be removed before turning on the power. Voltage checks should then be made using figure 6 (WD 1026) as a guide to insure that the above connections are properly made.

2.3.3 AC Power

The LS4157 is designed to operate from standard 120 volt, 60 Hz power line. The power cord plugs into the male receptacle in the rear panel of the decoder chassis. A three wire power cord is provided and it is recommended that the system not be operated without grounding. The AC line is fused with a 7 amp fuse located on the rear panel.

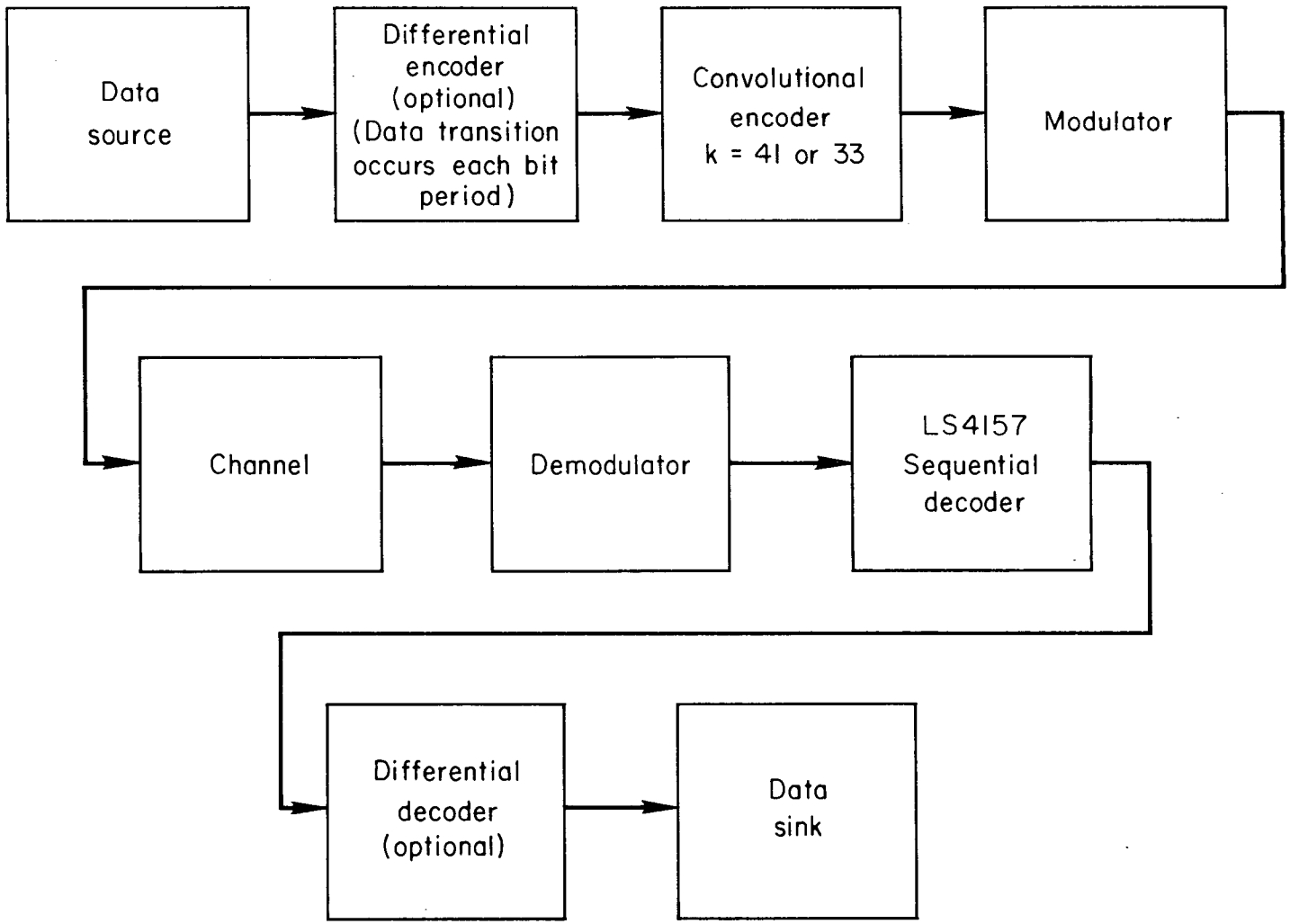


Figure 4. Communication system with the LS4157.

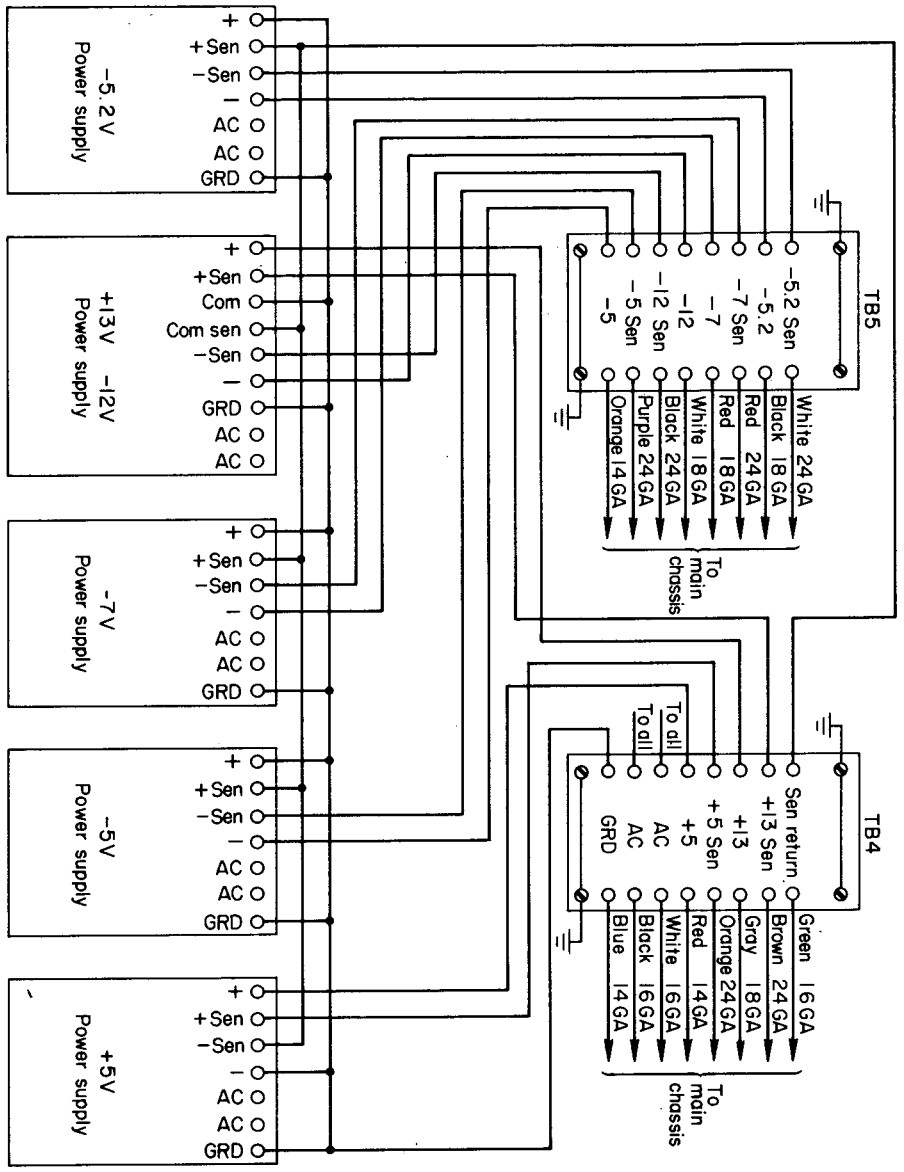
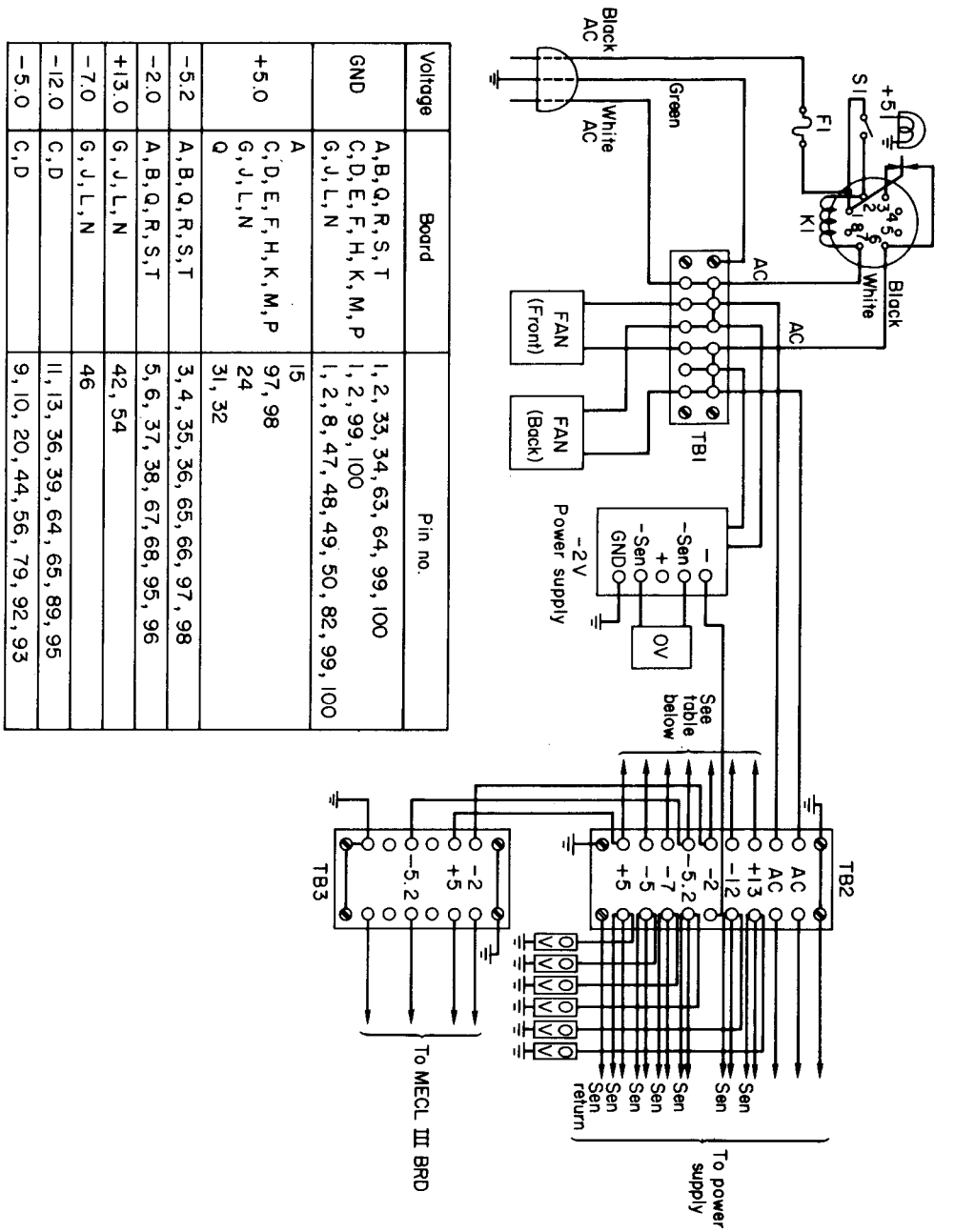


Figure 5. Wiring diagram for the power supply unit.



Voltage	Board	Pin no.
GND	A,B,Q,R,S,T	1, 2, 33, 34, 63, 64, 99, 100
	C,D,E,F,H,K,M,P	1, 2, 99, 100
	G,J,L,N	1, 2, 8, 47, 48, 49, 50, 82, 99, 100
+5.0	A	15
	C,D,E,F,H,K,M,P	97, 98
	G,J,L,N	24
	Q	31, 32
-5.2	A,B,Q,R,S,T	3, 4, 35, 36, 65, 66, 97, 98
-2.0	A,B,Q,R,S,T	5, 6, 37, 38, 67, 68, 95, 96
+13.0	G,J,L,N	42, 54
-7.0	G,J,L,N	46
-12.0	C,D	11, 13, 36, 39, 64, 65, 89, 95
-5.0	C,D	9, 10, 20, 44, 56, 79, 92, 93

Figure 6. Wiring diagram for the main chassis power.

2.3.4 Input/Output Signals

All input and output signal connections are made by means of miniature coaxial connectors on the front panel. The front panel is shown in figure 3. In all cases, 50 ohm cables should be used. The clock input is connected to the clock input terminal. The rate of the clock should be equal to the symbol rate. The clock and the data should be phased so that the data changes occur on the rising edge of the clock.

In serial mode the data is connected to the serial data input connector, and the serial parallel mode switch is placed in the serial position. In the parallel mode, the mode switch is placed in the parallel position and the two data lines are connected to the parallel input connectors. The order in which they are connected is unimportant. All input lines are terminated internally with 50 ohm resistors to -2 volts. Input signals should be compatible with ECL logic levels. Drivers should be capable of supplying 25 ma. in the logic one state.

There are three outputs: clock, data, and the error indication. The data clock will always be at the data rate regardless of whether serial or parallel mode is selected. The data output will have its transitions defined by the positive going edges of the data clock. The error indication output is normally logic 0 rising to a logic 1 when the output is likely to contain errors, and returning to the 0 state when the error condition terminates. The output drivers are MECL 10,000 compatible and are capable of driving a 50 ohm load terminated to -2 volts.

2.3.5 Interface Specifications

The fundamental specifications for the transmitter and receiver circuits are outlined in figure 7. These specifications apply whether a particular transmitter or receiver is used for data or clock signals. The decoder section requires either an R or 2R clock depending on whether the mode of the decoder is serial or parallel and outputs on R clock where R is the data rate. The decoder requires that the input clock and data have the timing relation shown in figure 7, i.e., data transitions can occur only at positive going transitions of the associated clock. The duty cycle of the input clock is not critical, however, a 50% duty cycle will be 50% in serial mode and will have the same duty cycle as the input clock in the parallel mode.

Transmitter*

Logic one	greater than −1.0 V (more positive)
Logic zero	less than −1.65 V (more negative)
terminated with 50Ω into	−2.0 V

Receiver

Logic threshold	−1.29 V
Input impedance	50Ω into −2.0 V

Clock timing relationship

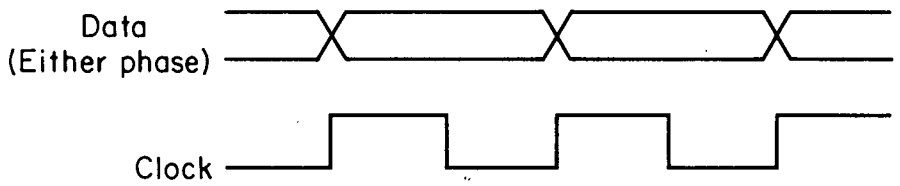


Figure 7. Interface specifications.

3. THEORY OF OPERATION

The theory of operation for the Hard Decision Sequential Decoder will be explained in two sections. The first section is a discussion of the decoder operation from a system block diagram approach (see figure 8). The next section gives more detailed information on the theory of operation. Detailed background information, of a general nature, is delineated in Appendix II.

3.1 System Discussion (use figure 8 as a reference).

A block diagram of the Hard Decision Sequential Decoder is shown in figure 8 (drawing 2-00155). The input buffer receives the input symbols from the channel in either serial or parallel form. If the input is serial, then it is converted into two parallel lines. One line represents the information bits and the other line represents the check bits. The information bits are clocked into a 65,000 bit-long shift register to delay them until the corrections are ready. The information bits and check bits are both fed into a syndrome generator (see Section 3.2) which generates the syndrome of the received symbols.

The syndrome passes into the I/O memory buffer where it is collected into 64 bit words and stored in the 65,000 bit Random-Access Memory (RAM). The memory is organized into 1024 words, 64 bits/word, and uses the AMS 6002 memory IC. Before a new word is written into a particular location in the RAM, the present contents of that location are read out and loaded into the I/O memory buffer, following which the new input word is written into the RAM. The word which was read from the RAM is the decoded information error sequence. This sequence is mod-2 added with the delayed information bits resulting in the corrected information bit stream.

When the CPU (the decoding logic) requests a new syndrome word from the RAM, a 64 bit word is read from the RAM into the CPU memory buffer. On the same cycle, the present contents of the CPU memory buffer are written back into the RAM in the same location. The 64 bit word read from the RAM is shifted into the CPU, 8 bits at a time, on demand from the CPU. This 8 bit word is converted from TTL logic levels to ECL logic levels and loaded into the CPU interface register.

The syndrome bits are then shifted out of the interface register one bit at a time into the fourth bit position of the syndrome corrector. The output of the fourth bit of the syndrome corrector, S4, is shifted into the algorithm logic. The algorithm logic determines whether: 1) to proceed forward or backward; 2) whether the present node contains an information error; 3) the amount by which the decoder metric should be changed. If the algorithm logic

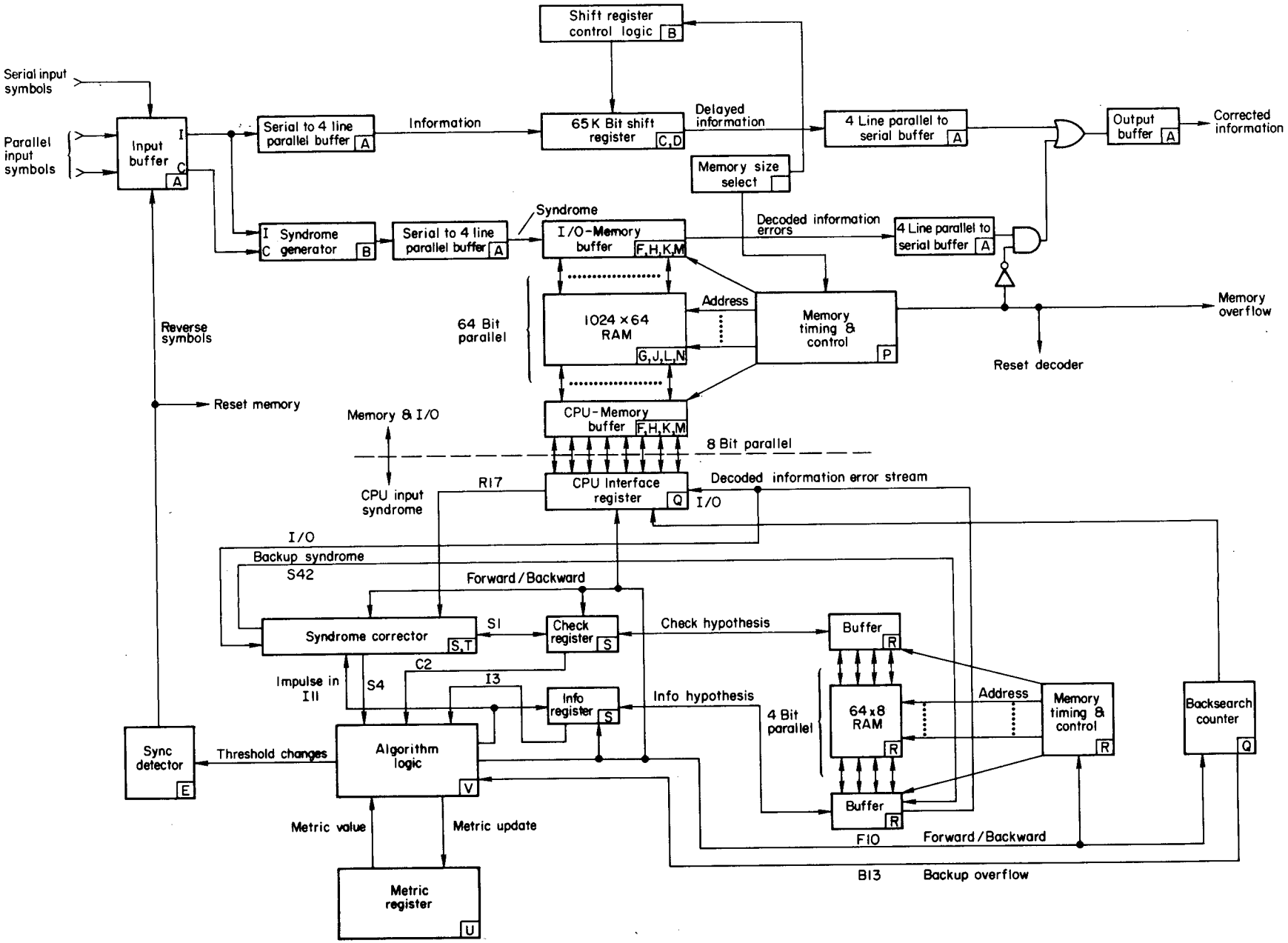


Figure 8. HDSD block diagram.

determines that the syndrome contains an information bit error, the syndrome is exclusive-ORed with the code connection vector, thus removing the effects of the information error.

The information and check bit hypotheses are shifted into a buffer where it is stored in a 64 x 8 bit RAM which serves as the backup buffer.

The backup buffer enables the decoder to backup and return to previous nodes in order to try alternate paths through the decoding tree. Before a new hypothesis word is written into the backup buffer, the present contents of the location to be written into are first read out. This word is shifted into the CPU interface register and is the decoded information error sequence.

When the CPU interface register has been filled with a new 8-bit word, it is loaded into the CPU memory buffer through the MECL-TTL interface. When a new 64-bit word is collected in the buffer, the memory is signalled that an access is required and the 64-bit word stored in the main RAM and a new 64-bit word are brought into the decoder.

When the decoder backs up, the syndrome bits that fall off the left side of the syndrome corrector are shifted into the right side of the information hypothesis backup buffer.

The decoder node synchronization is obtained by examining decoder threshold changes. If node sync is correct, then the decoder metrics are such that the rate of threshold tightenings will exceed the rate of threshold loosenings. If the node sync state is incorrect, the rate of threshold loosenings will exceed the rate of threshold tightenings. If the rate of threshold loosenings exceeds the rate of threshold tightenings for a long enough period of time, then a bad sync state is indicated. The sync detector outputs a signal to the input buffer which causes the interpretation of the channel input symbols to be reversed. The memory CPU address pointer is set equal to the I/O address pointer and the decoder attempts to resume decoding in the new sync state.

3.2 Design Concepts for the Hard Decision Sequential Decoder.

The LS4157 Hard Decision Sequential Decoder has been implemented as a syndrome decoder for a rate 1/2 systematic code. A received information bit and a received parity bit are input to the decoder at each bit time. To form the code syndrome, the received information bits are passed through a replica of the encoder and the generated parity bits are exclusive-ORed with the received parity bits. Figure 9 shows a representation of the encoder, channel, and syndrome calculator for a K=3 code. The noisy channel is modelled by the mod-2 addition of occasional errors (ones) to the encoder information and parity streams.

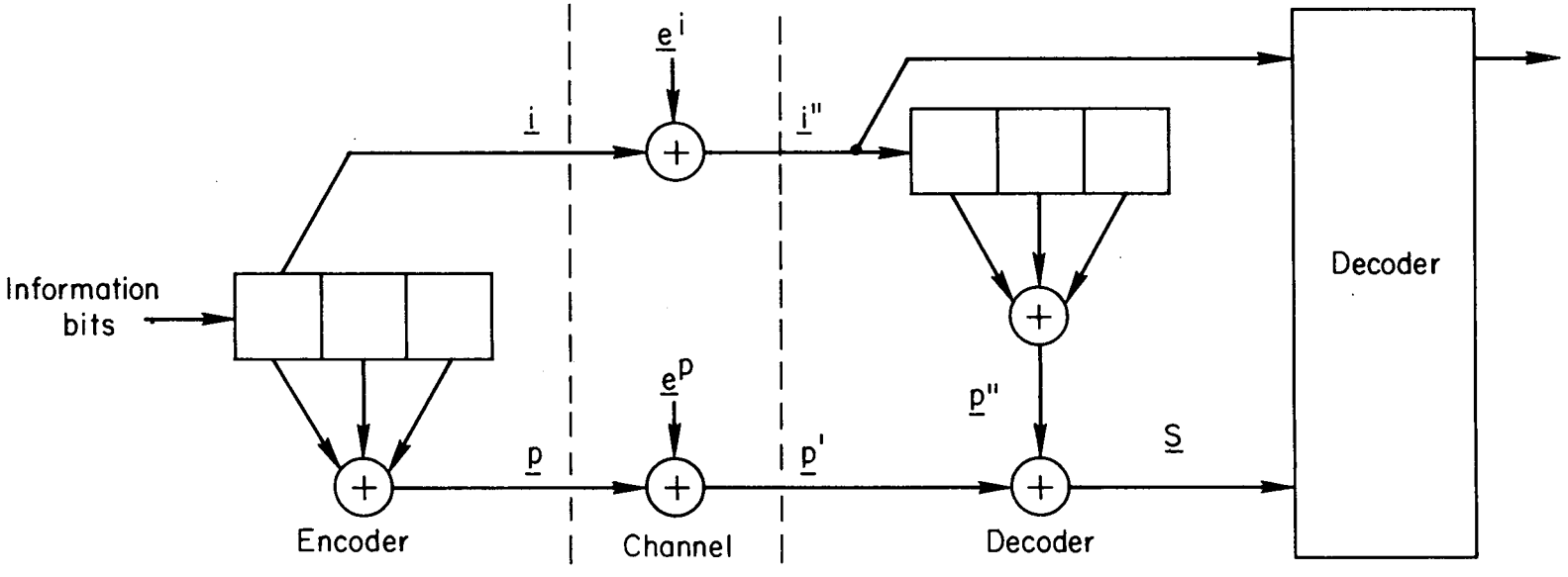


Figure 9. Communication system with the syndrome decoder.

Clearly, in the absence of noise, the syndrome bits input to the decoder are all zero regardless of the information sequence. This is because the parity bits generated in the syndrome calculator, $\underline{p}''$, and the received parity bits, $\underline{p}'$, are both equal to the actual parity bits, $\underline{p}$. Thus, since the code and the channel action are linear, the syndrome is a function only of the noise sequences. We can assume, therefore, without loss of generality, that the all zeros code sequence is transmitted.

This being the case, note that a single error in the information stream manifests itself in figure 9 as three consecutive 1's in the syndrome. In general, an information error causes the code generator to be exclusive-ORed into the syndrome. Each parity error, on the other hand, causes a single 1 to be exclusive-ORed into the syndrome.

It can be shown that putting the received data into the form of a syndrome is information lossless. A decoder operating on $\underline{s}$ can perform as well as one operating on $\underline{i}'$ and $\underline{p}'$. The function of a decoder operating on a syndrome sequence is to determine the most likely information and parity error sequences that could have resulted in that particular syndrome sequence. For a binary symmetric channel, this corresponds to determining the minimum weight error sequence consistent with the syndrome. The decoder forces the syndrome sequence to zero, by exclusive-ORing a "1" where it believes a parity error occurred, and the code generator similarly reacts where it believes an information error occurred.

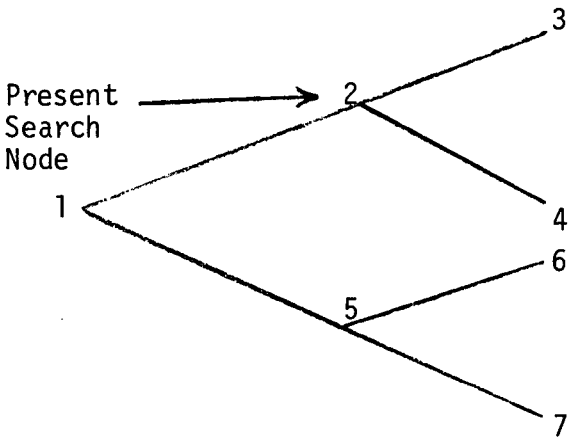
A syndrome sequential decoder keeps track of a metric as it "zeros" the syndrome. Each time it hypothesizes the occurrence of an error, the metric decreases. When it hypothesizes no error, the metric increases. If the decoder finds it has to correct too many errors in forcing the syndrome to zero, it will back up and change hypothesized information error decisions. Note that each information error decision affects the syndrome over a full constraint length.

Functionally, the syndrome decoder can be viewed as a box whose input is a syndrome sequence, and whose eventual output is an information error location sequence. This sequence is then used to correct errors in the received information sequence to form the decoder output.

The LS4157 incorporates two modifications to the basic Fano algorithm that improve computational efficiency. The first of these modifications is called "double quick threshold loosening." This scheme greatly reduces the number of short searches required. The

decoder can decode past all single isolated errors and nearly all isolated pairs of errors without initiating a backsearch. The technique capitalizes on code structure and a particular choice of branch metrics and threshold spacing by permitting the threshold to be lowered twice without a backsearch if the present value of threshold was reached by tightening twice.

The second new modification is called "diagonal steps." The technique of "diagonal steps" may be understood by considering the tree diagram below.



In the unmodified Fano algorithm, the decoder's attention is restricted to nodes 1, 2, 3 and 4 if the present search node is at node 2. The decoder could step forward to either node 3 or 4 or step back to node 1. If nodes 3 and 4 are both below threshold but node 6 or 7 is above threshold, the decoder must first step back to node 1, then forward to node 5, then forward to node 6 or 7 for a total of three steps. The diagonal step technique permits the decoder to go from node 2 to node 6 in only one step thus saving two computations. Furthermore, when moving forward, the modified algorithm always chooses the best node of 3, 4, 6, 7 to be searched first. If the branch of the tree stemming from node 6 is searched first but subsequently violates threshold, the decoder will return to node 5. Since the branches stemming from nodes 3 and 4 have not yet been searched, the decoder can step directly from node 5 to node 3 instead of getting there by first returning to node 1. This special "move" also saves two computations. The above technique is effective on short searches since the best nodes are always searched first, thus avoiding many back searches. The technique is also effective on long back searches since two computations are saved every time the decoder returns to the forward mode from the backward mode, a very frequent occurrence.

3.3 Algorithm Flow Chart

The Hard Decision Sequential Decoder algorithm is flow charted in drawing no. 2-000155. Suppose that the decoder is presently in the look forward mode. The present search node syndrome bit, F1, is tested. If F1 is a 0, the metric is tested for a possible threshold tightening. If the metric equals five, then the threshold is tightened by setting the metric to one. Since the threshold is being tightened, the quick threshold loosening flag, L, is incremented by 1, if less than 2. The decoder then steps forward and re-enters the look forward mode.

If syndrome bit F1 is equal to 1, then the previous node check bit, F2, is tested. If this bit is equal to 1, then we are in a situation in which it appears that the previous node contains an information error, since we have seen two syndrome bits in a row equal to 1. Since we have already taken the penalty for the error on the previous computation, we simply check whether the threshold may be tightened and increment the metric by one or tighten as required and step diagonally. The diagonal step is the same as the forward step, except that the connection vector is exclusive-ORed into the syndrome corrector. The decoder then re-enters the look forward node.

If the present syndrome bit, F1, equals 1 and the previous node check bit, F2, equals 0, then this node is a tie node. In order to take the tie, the metric must be greater than or equal to six. Since the metric is decreased by five on nodes that contain a single error, if the value of the metric is greater than or equal to six, then subtracting five will permit the metric to remain greater than or equal to one. A metric of zero or less is a threshold violation. If the metric is greater than or equal to six, then five is subtracted from the metric and the decoder steps forward. If the metric had been less than six, then the quick threshold loosening indicator bit, L1, is tested. If L1 is equal to 1, then the threshold may be lowered. Since the threshold spacing is equal to five and we are at a tie node which results in a reduction in metric by five, the net result will be no change in the metric. The quick threshold loosening indicator is reduced by one and the decoder steps forward and re-enters look forward mode. If L1 had been equal to zero, then both of the available quick threshold loosenings have already been used and there is no way to proceed forward without violating threshold. Since F2 is equal to zero, we know that the previous node must have been a good node and we incremented the metric to get to our present position. Therefore, 1 is subtracted from the metric and the decoder steps back and enters the look back mode. It should be noted that the decoder always steps forward along the upper branch of the tree in a step forward mode. The upper branch of the tree corresponds to assuming

that there is no information error on the present node. All changes in this assumption are accomplished by diagonal steps, i.e., either the diagonal steps that appear in a look forward mode or the diagonal steps that appear in a look back mode.

In the look back mode, B13, the backup overflow indicator is tested. If B13 is a 1, the backup buffer has overflowed. It is then necessary to lower the threshold and re-enter the look forward mode. In order to do this, however, we must look at the present node syndrome bit, F1, to determine the change in the metric. If F1 is equal to 0, then the metric is incremented by 1. The threshold is not loosened directly, but the quick threshold loosening flag, L, is incremented by 1 so that the first time that the decoder violates threshold on the following forward move, the threshold will be lowered. If, on the other hand, the syndrome bit F1 is equal to 1, then the present node is a tie node, and the threshold may be lowered by simply not changing the metric. The decoder then steps forward and re-enters the look forward mode.

If we are not in a backup overflow situation, then B13 will be equal to 0. We then test bit F6, the previous node syndrome bit. If F6 is equal to 1, then we test the present syndrome bit F1. If this bit is also equal to 1, there are no possible ways to re-enter the look forward mode. Since we are on a tie branch, when we backup we must increment the metric by 5. If F1 was a 0, however, we do have an alternate path available provided that the metric is greater than or equal to 6. We test for this situation, and if it is present, then we may re-enter the look forward mode after subtracting 5 from the metric. Otherwise we add 5 to the metric and step back.

If bit F6 had been equal to 0, we test bit F2, the previous node check bit. If F2 is equal to 1, then we are looking back into a node where we hypothesized a double error. There is no way to turn around and proceed forward since all available nodes forward from this point have been searched. We must, therefore, step back and add 11 to the metric which was the penalty for the double error on the forward move. If F2 is 0, we must then test to see if we may lower the threshold. We may lower the threshold if the metric is presently equal to 1. If the metric is equal to 1, we lower the threshold then by setting the metric equal to 7. We then step forward and re-enter the look forward mode. If the metric is not equal to 1, we test the present syndrome bit F1.

If F1 is a zero, the only available forward moves involve accepting a double error penalty on the previous node, plus a tie penalty on the present node. In order to do this, the metric must be greater than or equal to 18. If it is, we then subtract 17 from

the metric and take a diagonal step. If it is less than 18, we have no forward move available, and we subtract 1 from the metric and backup.

If the present syndrome bit, F1, is equal to 1, then our only forward move requires a double error penalty on the previous node and a good node metric at the present node. The metric must be greater than or equal to 13. If it is not, we subtract 1 from the metric and backup. If it is, we must check for the possibility of a threshold tightening in this case, since the effective move here is to backup 1, proceed forward along the lower branch, and then proceed forward along the upper branch. It is possible for this to involve a threshold tightening if the present value of the metric is equal to 17. If the metric is not equal to 17, we subtract 11 from the metric and take a diagonal step. If the metric is equal to 17, we set the metric equal to 1 and increment the quick threshold loosening flag, L, by 1 and take a diagonal step.

4. DETAILED CIRCUIT OPERATION

The schematics are located in Appendix III and the wire list in Appendix IV. Card locations are summarized in figure 10.

4.1 Input/Output Board, Location A, Schematic 4-000172

The incoming signals and the clock are buffered into the decoder using a MECL 10,115 quad line receiver. The coaxial input lines are terminated in 50 ohm resistors to -2 volts at the inputs to the line receivers. The incoming data is then passed through a set of gates which format the signals according to the serial/parallel control switch. If the data input is serial then the data is clocked serially through the three flip-flop register. If the input is parallel, then bit 2 is clocked into the middle flip-flop and bit 1 is clocked into the first flip-flop and into the third flip-flop in complemented form. (This is to provide the appropriate function in case the parallel input is from a QPSK modem.) The output of the three flip-flop register is then passed through gates and clocked into two flip-flops for output. The intermediate set of gates is used to determine node sync. In one sync state the bits are taken from the first and second flip-flops, and in the other sync state they are taken from the second and third flip-flops. The information bits are then converted from serial format to a four line parallel format, converted to TTL levels, and passed on to the information bit memory. The information bits and check bits are also fed to the syndrome generator. The syndrome is returned to the I/O Board, where it is converted to four line parallel format, converted to TTL levels, and passed on to the main memory buffer

Card Location	Card Type
A	Input/Output
B	Syndrome Generator
C	Information Memory Shift Register
D	Information Memory Shift Register
E	Information Memory Control
F	Main Memory Buffer
G	Main Memory
H	Main Memory Buffer
J	Main Memory
K	Main Memory Buffer
L	Main Memory
M	Main Memory Buffer
N	Main Memory
P	Main Memory Control
Q	Backup Counter and Interface
R	Backup Buffer
S	Syndrome Corrector #1
T	Syndrome Corrector #2
X	Algorithm Logic

Figure 10

boards. In serial mode, the input symbol clock is divided by two in IC 49. The data rate clock is then divided by four in IC 9, converted to TTL levels, and passed on to the Information Bit and Main Memory.

The delayed information bits from the Information Bit Memory are converted from TTL to ECL logic levels and converted from four line parallel to serial format. The delayed information bits are brought out inverted to TPB. The delayed information bits are then mod-2 added with the error sequence, reclocked in IC 19, and passed through a line driver to the data output connector.

The information error sequence from the Main Memory is converted to ECL logic levels and from four line parallel to serial format. They are brought out inverted on TP 10. The information error sequence is then passed through an 8-bit shift register, gated with the error indicator and then mod-2 added with the delayed information bits.

The error indicator bit from the Main Memory control board is converted to ECL levels, gates the information error sequence, is reclocked and then buffered through a line driver to the output connector.

4.2 Syndrome Generator, Location B, Schematic 4-000157

The syndrome generator encodes the received information bits. The generated check bits are mod-2 added with the received check bits to form the syndrome.

The encoder is a duplicate of that which is used in the transmitter. Two constraint lengths are provided, K=33 and K=41. The connection vector for the code is 71547370131746, expressed octally for K=41. The K=33 code is the truncation of the K=41 code.

The syndrome generator is implemented using MECL MC 10131 flip-flops with MC 10107 mod-2 adders connected between the appropriate stages. The inverted syndrome is brought out to TP 5.

4.3 Information Memory Shift Registers, Locations C and D, Schematic 4-000160

Each of the two memory boards contains two identical circuits. The four line parallel information bit stream is converted to 16 line parallel by IC's A1 - A2, and B1 - B2 on the two memory boards. Each of the 16 lines is then delayed by a 4096 bit MOS shift register.

Each 4096 bit shift register consists of three 1024 bit registers and a quad 256 bit register. Taps are provided at 256, 512, 1024 and 2048 bits so that the memory size can be reduced. (Reduction in memory size is primarily for test purposes.) The appropriate tap is selected by a multiplexer which is controlled by the memory size switch. The 16 line parallel shift register outputs are converted back to 4 line parallel by IC's A28 - A29 and B28 - B29 on the two boards. The 4 line parallel outputs are available on TP4 and TP10.

In the high speed mode, each of the sixteen 4096 bit shift registers is clocked at 1/16 of the data rate. Since the shift registers have a minimum guaranteed speed of 10 kHz, the high speed mode may be used with confidence at data rates down to 160 kBPS. For practical purposes, however, at 25°C ambient temperature, the shift registers work satisfactory at much lower speeds. In the high speed mode, the data simply shifts straight through the memory.

In the medium speed mode, each of the shift registers is clocked at the data rate and each data bit is circulated through the memory 16 times. Smaller memory sizes than 4096 bits are provided by circulating the data through eight times or four times for 2048 and 1024 bits, respectively.

In the low speed mode, the shift registers are connected in a fully recirculating mode. A counter on the memory control board keeps track of the read/write point in the register. The data is recirculated by a 5 MHz clock.

4.4 Information Memory Control, Section E, Schematic 4-000159.

The data clock is divided by 4 on the I/O board. The result is again divided by 4 by IC 19. The shift register clock pulses are generated by IC's 29, 20 and 9. Memory size and data rate range switch positions are stored in IC's 1, 2 and 3. IC's 18 through 28 control the memory timing in the low speed mode. The remaining logic on sheet 1 generates various timing and control signals for the shift registers.

The node sync counter is also located on this board and is shown on sheet 2 of drawing 4-000159. IC's B2 - B5 form an up/down counter which is counted up on threshold tightenings and down on threshold loosenings. When the most significant eight stages reach all ones, the counter is prevented from counting up. If the counter underflows, the state of the node sync flip-flop, IC B7, is changed. Threshold tightenings that occur when the error indicator is on are ignored.

4.5 Main Memory

The main memory section contains a total of 9 circuit boards, one for the memory control logic, four identical memory boards, and four identical buffer boards. The control board plugs into card slot P; the memory boards into locations G, J, L, N; and the buffer boards into locations F, H, K and M.

The main memory provides up to 65k bits of storage for syndromes and the decoded information bit error sequence. The total delay through the memory and decoder may be reduced from 65k down to 1k bits in seven steps. The basic storage element is the AMS 6002, 1024 bit random access memory IC. The memory contains 64 of these IC's and is organized into 1024 words with 64 bits per word.

The memory has two asynchronous ports, one for I/O and one for the decoding logic. Data from the I/O section and from the decoding logic is buffered into 64-bit words for the main memory by TTL shift registers. The data from the I/O section is received in 4-bits parallel format by the main memory and converted back to 4-bit parallel for delivery to the output section. The interface to the decoding logic is 8 bits parallel due to the high operating rate of this section.

Control logic provides either the I/O section or the decoding logic section the memory cycles as they are required. Additional buffering is provided to allow for the delay that may be required due to a cycle in progress. One full 64-bit word is buffered for both the I/O and the decoding to allow this asynchronous operation.

4.5.1 Main Memory Board, Location G, J, L, and N, Schematic 4-000148

Each memory board contains 16 AMS 6002 random access memory (RAM) integrated circuits (IC). Associated with each RAM IC is a sense amplifier and write driver circuit. The sense amplifier is an MC1414 dual sense amplifier IC. The schematic of the typical write driver is shown as circuit A on the drawing. The circuit consists of two level shifters and inverters: To write a logic zero, Q1 is turned on; to write a logic one, Q2 is turned on.

The ten address inputs, MA0F through MA9F, are buffered by TTL inverters and then converted to MOS levels by circuit B, the address driver. The reset input, RESF, and the clock input, MCLKF, are also buffered by TTL inverters and converted to MOS levels by circuits C and D. These circuits are similar to the address drivers, circuit B, except that emitter followers are added to provide more capacitance drive capability.

4.5.2 Main Memory Buffer, Locations F, H, K, and M. Schematic 4-000164

Each main memory buffer board contains a 16-bit slice of the I/O buffer, the decoder logic buffer and the write select gates. The I/O buffer consists of a 16-bit serial to parallel converter, a read holding buffer and a write holding buffer. IC's 21 and 22 form the serial to parallel converter.

The circuit effectively converts the serial input to a 2-bit parallel input since the shift registers are clocked on alternate clocks as controlled by signals INHA and INHB. When new syndrome data is shifted into the shift register, the decoder information error sequence is shifted out. The shift registers outputs are multiplexed together by IC 25. The result is fed to the I/O board and brought out to TP1.

While the information is shifting through the shift register, a memory cycle is requested. When the cycle is granted, the data read from the memory is loaded into the I/O read holding register, IC's 5, 6, 7 and 8. After the read part of the memory cycle, the data in the I/O write holding register (IC's 9, 10, 11 and 12) is selected by the write gates (IC's B1 through B16) and is written into the memory.

After the shift registers are each clocked eight times, the shift register contents are loaded into the write holding register and the contents of the read holding register are loaded into the shift register.

The CPU buffer registers operate in a similar manner.

4.5.3 Main Memory Control, Location P, Schematic 4-000158

Timing signals for the memory cycles are generated by IC's A2, A3, and their associated timing resistors and capacitors. This circuit provides five independently adjustable time intervals. The operation of the circuit is similar to the "twisted ring counter" (or "Johnson Counter" where the complement of the last stage is fed back into the input) except that it is self clocking.

The clock from the CPU (which is the computation rate clock divided by 8) is counted by a 3-bit counter which indicates when the CPU buffer shift register has been emptied by the CPU. When the counter overflows, the carry term sets the CPU request flip-flop.

The clock from the I/O board (which is the data clock divided by 4) is counted in a 4-bit counter which indicates when the I/O shift register has been emptied. When the counter overflows, the I/O request flip flop is set. Every time an I/O cycle is taken, a 50 μsec, retriggerable one shot is triggered. Should the one shot time out (only at lower data rates) a refresh cycle is requested.

The three possible requests (CPU request, I/O request, and refresh cycle) are ORed together and any request will start a new cycle by triggering the timing circuit immediately upon completion of any previous cycle.

The contents of the request flip-flops are then loaded into a 3 flip-flop register which drives a priority network. The priority network resolves simultaneous requests, first in favor of the CPU and then in favor of the I/O.

Three address counters are provided, one for I/O, one for CPU, and one for refresh. Note that only a 5-bit address counter is necessary for refresh. When the CPU and I/O counters reach all ones, they are loaded with a number determined by the setting of the memory size switch.

When a cycle is started, the output of the priority network selects the appropriate address and loads it into the address holding register. If the CPU address and the I/O address become equal then the unit is either in an overflow or an underflow situation. An overflow situation exists if the last memory cycle was an I/O cycle. Underflow is indicated if the last cycle was a CPU cycle. When underflow occurs, the CPU request must be blocked since the data has not yet been input to the decoder. When the CPU request flip-flop is set and the CPU buffer shift register becomes half empty, the CPU computation clock is gated off by CPUNT until the present CPU request is honored and the new data is available in the CPU read holding register.

When an overflow occurs, the present I/O cycle request is blocked and the next two cycles are given to the CPU. Also, the internal states of the CPU are reset and the CPU buffer registers are cleared. The error counter is enabled which turns on the error indicator and disables corrections for the next 420 output bits.

When the clear button is depressed, the states of the controller are reset and the I/O and CPU address counters are set equal. The decoder is then placed in an overflow condition. The error counter is disabled until the I/O address counter cycles through all its addresses and the new input data reaches the output.

4.6 CPU Backup Counter and Interface, Location Q, Schematic 4-000151

The function of the backup counter is to determine when the decoder is moving forward to new nodes and to detect backup buffer overflow. An up/down counter is used to provide this function. The counter is identical to the backup buffer address counter. The least significant stages of the counter, B1 and B2, are a mod-4 shift counter. The most significant stages, B3 - B8, are a mod-63 linear shift register generator. When the counter reaches the zero state in the forward mode, flip-flop B12 is set, which indicates that new nodes are being reached. (Note that the "zero" state is defined as 010000 for B3 - B6.) When the counter reaches this state in the backward mode, a backup overflow is indicated by B13.

The memory interface circuit is an 8-bit parallel to serial converter with TTL to MECL and MECL to TTL level converters. Whenever the decoder progresses forward eight new nodes, an eight bit word from the main memory buffer is converted to MECL logic levels by the resistor networks, R_t, and loaded into the eight bit shift register R1 - R8. At the same time, the present contents of R1 - R8 are loaded into R9 - R16. The contents of register R9 - R16 are converted back to TTL logic levels and shifted into the main memory buffer.

The computation clock is divided by eight when moving forward to new nodes to generate CPCLK, which is converted to TTL levels and sent to the main memory control board.

The main memory overflow signal, CPOVT, is converted to MECL levels, buffered and sent to the other CPU boards, converted back to TTL levels and returned to the main memory control board as OVACNT.

4.7 Syndrome Corrector #1, Location S, Schematic 4-000152

The syndrome corrector is a right-left shift register with mod-2 adders located between the appropriate stages in accordance with the code. The first 22 stages of the syndrome corrector are on board #1. The remaining stages are on syndrome corrector #2.

The incoming syndrome bits are exclusive ORed into the register at stage S4 when proceeding forward to new nodes. The corrected syndrome at stage S4 is sent to the Algorithm Logic board when moving forward.

The contents of the syndrome corrector stage C1 is the check bit hypothesis. When moving forward, these bits are shifted into the backup buffer. When backing up, they are returned to the syndrome corrector.

The information error hypothesis, F11, is also stored in the backup buffer when moving forward to new nodes. When backing up, they are returned to the syndrome corrector.

When backing up, the syndrome corrector also provides the information hypothesis, I3, and check hypothesis, C2, to the Algorithm Logic board.

4.8 Syndrome Corrector #2, Location P, Schematic 4-000153

This board contains stages S23-S42 of the syndrome corrector. The operation is identical to the circuitry on syndrome corrector #1.

When the decoder backs up, the syndrome bits that shift out are stored in the information hypothesis half of the backup buffer. When returning in the forward mode, these bits, I10, are shifted back into the syndrome corrector. When moving forward to new nodes, zeroes are shifted into S42.

The constraint length switch shortens the constraint length to 33 by bypassing stages S34-S41.

4.9 Backup Buffer, Location R, Schematic 4-000154

The function of the backup buffer is that of a 2 bit wide, 259 bit long, right-left shift register. The shift register function is actually performed by eight 64-bit random access memory IC's that are addressed by an up/down counter.

The address counter, A1 - A10, operates identically to the back search counter previously described.

Consider the operation of the information hypothesis half of the backup buffer shown on sheet 2 of the schematic. The information hypothesis stream, I3, from the syndrome corrector are shifted into the right-left-parallel load register I4 - I10. When four new bits have been shifted into I5 - I8, they are loaded into the write holding register I11 - I14. At the same time, the four bits read out of the present address of the RAMs, Z5 - Z8, are loaded into I7 - I10. On the next clock pulse, the contents of I11 - I14 are written into the memory. No memory operations are performed on the next clock time to allow for the write pulse recovery time. The address is advanced on the next clock pulse. On the next clock pulse, the read and register load operations are repeated since four new bits have been shifted into I4 - I10. The output is taken from I10.

The operation in the backward mode is similar except that register I11 - I14 is loaded from I6 - I9 and data read out of the memory is loaded into I4 - I7. The output in this case is I4, which is sent back to the syndrome corrector.

Operation of the check hypothesis half of the backup buffer is similar but simpler since the check hypothesis is thrown away when advancing forward to new nodes.

4.10 Algorithm Logic, Schematic 4-000156 (This board is clamped in place at the end of the card cage.)

The computation clock is generated by the delay line oscillator composed of IC 1 and a length of coaxial cable. The oscillator oscillates at twice the computation clock rate and is divided by two in IC 2. The signal CPUNT is reclocked by IC 3 and gates off the computations clock when CPUNT is true. The resulting gated clock drives a high fanout clock distribution network. The computation clock is divided by 128 by IC's 10 - 14 when the clock rate switch is in its low speed position.

The syndrome bit, S4, from the syndrome corrector is exclusive ORed into F1, the present node syndrome bit. This signal is developed in three parallel flip-flops in order to obtain sufficient fanout. Signal F2 is the previous node check bit and signal F6 is the previous node syndrome bit.

The branch metric is stored as a three digit number. For ease in decoding, the least significant digit is mod 6, the middle digit is mod 3, and the most significant digit is mod 6. In other words, the metric is equal to $C_1 + 6C_2 + 18C_3$ where C_1, C_2, and C_3 are the least, middle and most significant digits, respectively. The least significant digit is stored in M1 - M3, which is a right-left-hold, twisted ring counter. The middle digit is stored in M6 - M8 which is a right-left-hold ring counter which circulates a single one. The most significant digit is stored in M9 - M11 and is a right-left-hold twisted ring counter. Flip-flop M12 is true when the most significant digit is not zero.

IC's 45 - 72 and 79 - 82 cause the decoder to follow the algorithm flow chart (drawing 2-000155). The flow chart may be described by a set of equations which are implemented with these gates. Signals G1 - G12 and G30 - G35 are commonly used partial products of these equations. The signal G13 controls the forward-backward motion of the decoder. Signal G26 is true for diagonal steps forward. Signals G16, G17 and G18 control the middle digit of the metric. Signals G21, G22 and G23 control the most significant digit. Signals G13, G14 and G15 control the least significant digit.

5. MAINTENANCE

No periodic maintenance is required for the sequential decoder. Fault isolation procedures are outlined below should difficulties be encountered with the decoder. The power supply voltages should be checked first if the decoder is not operating satisfactorily. If the voltages are within the specified limits (Table I), procedures noted below should be followed.

TABLE I

Voltage (Volts d.c.)	Limits
+13.0	+12.4 to +13.6
+ 5.0	+ 4.8 to + 5.2
-12.0	-11.4 to -12.6
- 7.0	- 6.6 to - 7.4
- 5.2	- 4.8 to - 5.6
- 5.0	- 4.8 to - 5.2
- 2.0	- 1.9 to - 2.1

5.1 Preliminary Tests

The required equipment includes: a PN data source, a convolutional encoder, a digital noise generator, and an error detector. The procedure is as follows: first connect the data source, encoder and error detector to the decoder and verify that an error-free data input results in error-free data output. Note that sufficient time must be allowed for the decoder to establish node sync and for data to pass through the decoder. After node sync has been established, the decoder error indicator light should go out and remain out. If the decoder fails this test, refer to paragraph 5.2.

If the decoder passes the above tests, add the digital noise generator to the test setup. For input error rates less than 1%, output errors and overflow events should be very rare. As the input error rate increases, the output error rate and overflow rate will increase. For input error rates over 5%, the decoder will be

in the overflow state most of the time. Note that sequential decoders are extremely sensitive to correlation in the noise. At an input error rate of 3%, the output error rate should be less than 10^{-5} at high data rates with 65k memory. Note that the output errors occur in bursts. (Single error events are rare even at high input error rates.) If the decoder fails these tests, then turn to paragraph 5.3.

5.2 Decoder Fails to Pass Error Free Data

5.2.1 Error Indicator Light On

First check the test point on the Syndrome Generator board (slot B). This point is the inverted syndrome and should be at the one state (MECL levels) with error free data. If not, then first check the test configuration. If the configuration is OK, then the problem is probably on the syndrome generator board. Other likely possibilities include the input section of the I/O board (slot A), and the node sync circuitry on card E. A subtle problem in the main memory or CPU could also result in this behavior.

If the syndrome test point is OK, but the error light remains on, then the problem is most likely in the main memory or CPU. Another possibility is the syndrome serial-to-four-line parallel converter on card A. Next check test points 2 and 11 on Main Memory buffer cards, in slots F, H, K, and M. These points should be all zeroes (TTL levels). If not, then the associated memory card or the buffer card is faulty. Check the memory card by interchanging it with the spare card. Check buffer card by interchanging with another buffer card. If the problem moves with the card, then the buffer board is faulty.

5.2.2 Error Indicator Light Off

First, check test point 10 on Card A. This is the inverted information bit error sequence which should be all ones (MECL level). If not, then the problem is most likely in the main memory or CPU. Check memory as in section 5.2.1.

If TP10 is OK, then the problem is probably in the information bit memory. Check TP10 and TP4 on both information memory cards (slot C and D). Each of these test points has every fourth bit of the input information sequence. If the problem is seen on any of these test points, then the problem has been isolated to either the right or left half of one of the boards. In order to locate the problem precisely, the board must then be extended. To isolate the problem to a particular bit slice, check pins 2, 3, 4 and 5 of IC's A29 or B29.

If difficulty is experienced locating the problem using the PN data, use the all "zeroes" data with digital errors or a fixed pattern data generator using a low density of "ones".

5.3 Decoder Passes Error Free Data but the Output Error Rate Is Too High

If the decoder passes all tests in section 5.2, then most I/O board functions, the Syndrome Generator, and the Information Bit Memory are probably functioning properly. The problem is therefore in the CPU or the main memory.

5.3.1 Main Memory Tests

If there is a problem in the main memory, then the output single error probability will be too high. The oscilloscope can be used as a correlator to isolate the problem. The most likely problems are a defective address driver or a defective memory IC.

A defective address driver can usually be isolated by syncing the scope to the signal on TP13 of the main memory control board (card P). This signal is the carry out of the I/O address counter. Then check TP1 on each of the main memory buffer boards. (This signal is every fourth bit of the information error sequence.) If one of the test points shows a significant correlation of errors, then the associated memory board probably has a faulty address driver and should be replaced.

A defective memory IC can usually be discovered by repeating the above test with the scope synced on TP12 of the main memory control board. This signal is a pulse at the beginning of each I/O memory cycle. If a significant correlation of errors is discovered on one of the buffer board test points, then the associated memory board probably contains a defective memory IC and should be replaced.

5.3.2 CPU Debug

A special test setup has been devised for checkout of the CPU since the CPU is very difficult to debug with regular input signals. The inputs to the decoder are set up to generate an all ones syndrome. This is done by putting the decoder into PSK-Parallel mode. One of the parallel inputs is grounded and the other is left open. An input clock is provided at any convenient data rate, preferably about 1 MBPS.

The decoder is unable to decode an all ones syndrome and will continually overflow (thus turning on the error indicator).

An oscilloscope is synced to the overflow signal at the connector labeled OVFL on Syndrome Connector #2 (card T). The signals at jacks EOR and FOR on the same board are then observed. Note that the signals on these connectors have been series terminated and may be connected to the oscilloscope inputs with an unterminated 50Ω coaxial cable. The signal FOR is true (MECL levels) when moving forward. The signal EOR is true when syndrome corrector is EORed with the code connection vector. This signal is true whenever the decoder takes a diagonal step when moving forward or steps back from the lower branch of the tree.

Since the overflow resets the main memory buffer, the first group of syndrome bits will be zeroes. The syndrome will then become all ones, thus causing the decoder to begin searching. Eventually, the decoder will again overflow and the cycle will repeat. The correct decoder operation may be determined by comparing the algorithm flow chart sequences with the actual decoder operation. When a discrepancy is revealed, the cause can be traced, thus yielding the faulty condition.

The MECL III board may be extended easily for debugging procedures. Simply loosen the two nylon screws which hold the board in place and slide out the board. Then screw in the nylon screws all the way and slip the board back in the slot. The board will then rest on the screws in an extended position.

APPENDIX I

DIGITAL NOISE GENERATOR

This report describes the technique used for generating very high speed, hard decision, pseudo-random noise suitable for testing and evaluating high speed decoders. The purpose of the noise generator is to generate 9-bit independent random numbers at the symbol rate (symbol rate is twice the data, e.g., if the data rate is 60 megabits per second, the symbol rate is 120 megabits per second).

The method chosen for the high speed digital implementation uses a PN generator. The PN generator is clocked 9 times for each 9-bit number produced. Each 9-bit number is thus completely disjoint from every other number. The problem encountered with this technique is that the PN generator must be clocked at a rate of $9 \times 120 \times 10^6$ or 1.08×10^9 times per second -- clearly out of the question for even MECL III logic devices.

The solution for the above problem is discussed in the following paragraphs. The proposed circuit generates discrete segments consisting of disjoint 9-bit PN sequences during each clock time. During this time, signals propagate through only one gate delay and one flip-flop.

Consider the 41 stage PN generator shown in figure I-1. After each clock time, the new contents of state 1 is the mod-2 sum of the old contents of stages 38 and 41. All other stages shift right by 1. Let us examine what the generator will contain after 9 clock times.

For this purpose, let s_i, $1 \leq i \leq 41$, be the initial contents of the i^{th} stage. Let t_i be the content after 9 shifts.

Clearly,

$$
\begin{aligned}
t_{41} &= s_{32} \\
t_{40} &= s_{31} \\
&\vdots \\
t_{10} &= s_1 \\
t_9 &= s_{41} \oplus s_{38} \qquad \text{(Eqn. 1)} \\
t_8 &= s_{40} \oplus s_{37} \\
&\vdots \\
t_1 &= s_{33} \oplus s_{30}
\end{aligned}
$$

This implies the implementation shown in figure I-2. This circuit consists of five 5-bit shift registers, four 4-bit shift registers, and nine exclusive-OR gates. It realizes equation 1. In each clock time, a new vector $(t_1, t_2, \ldots, t_9)$ is obtained. The numbers in the memory elements correspond to those in figure I-1.

The 9-bit number, $t = t_1, t_2, \ldots, t_9$ which is uniformly distributed between 0 and 2^9-1, can now be compared with a fixed 9-bit number, b, to determine whether or not a channel output error should be generated.

If $t < b$, a symbol in error is output; otherwise, a correct symbol is output. A "0" means no error and a "1" denotes an error. The output error probability will be $p=b/2^9$.

The comparison process is basically a subtraction, t-b, where there is a carry out if $t > b$. Generating the carry for the subtraction of 9-bit numbers is a complex function to realize in a few gate delays. However, if we compare b against the number formed by taking successive bits of successive t's instead of each t itself, the comparison can be done easily by the pipelining process shown in figure I-3. Here C denotes a carry generator (or a one bit adder with carry in) which outputs a "1" if two or more of its inputs are "1". This function can be implemented with three 2-input gates in one logic level. The flip-flops delay each of the intermediate results to effect the pipelining.

All flip-flops use a common clock, which is the symbol clock. The maximum clock rate would be 120 MHz, which is well within the capabilities of MECL III.

The statistics of the disjoint 9-bit numbers have been verified through sequential decoder simulations (computer software programs). The distribution of decoding computations was within 0.1 dB of theory and thereby verifies the pseudo-random noise output.

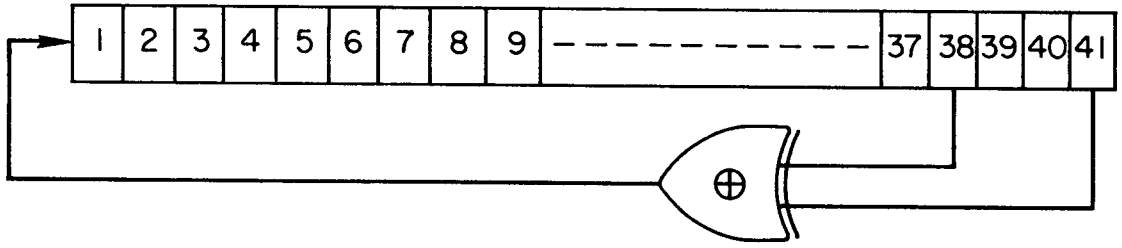


Figure I-1. 41-stage trinomial PN sequence generator.

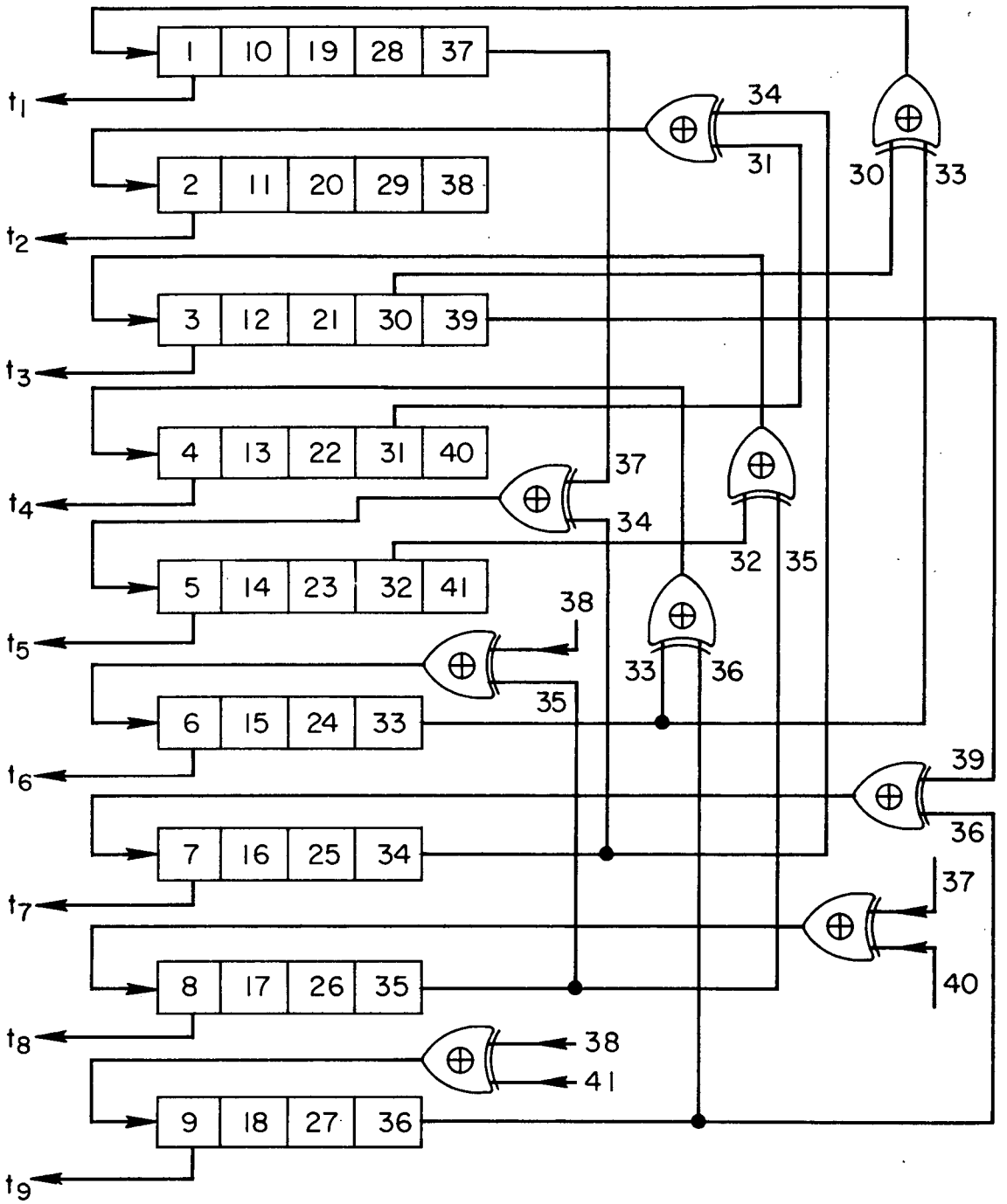


Figure I-2. Noise generator for the output of disjoint 9-bit segments of a PN sequence in one clock period.

Notes: Shift register numbers refer to the equivalent stages of the 41-bit serial shift register of figure I-1.

This circuit realizes equation 1 for the noise generator.

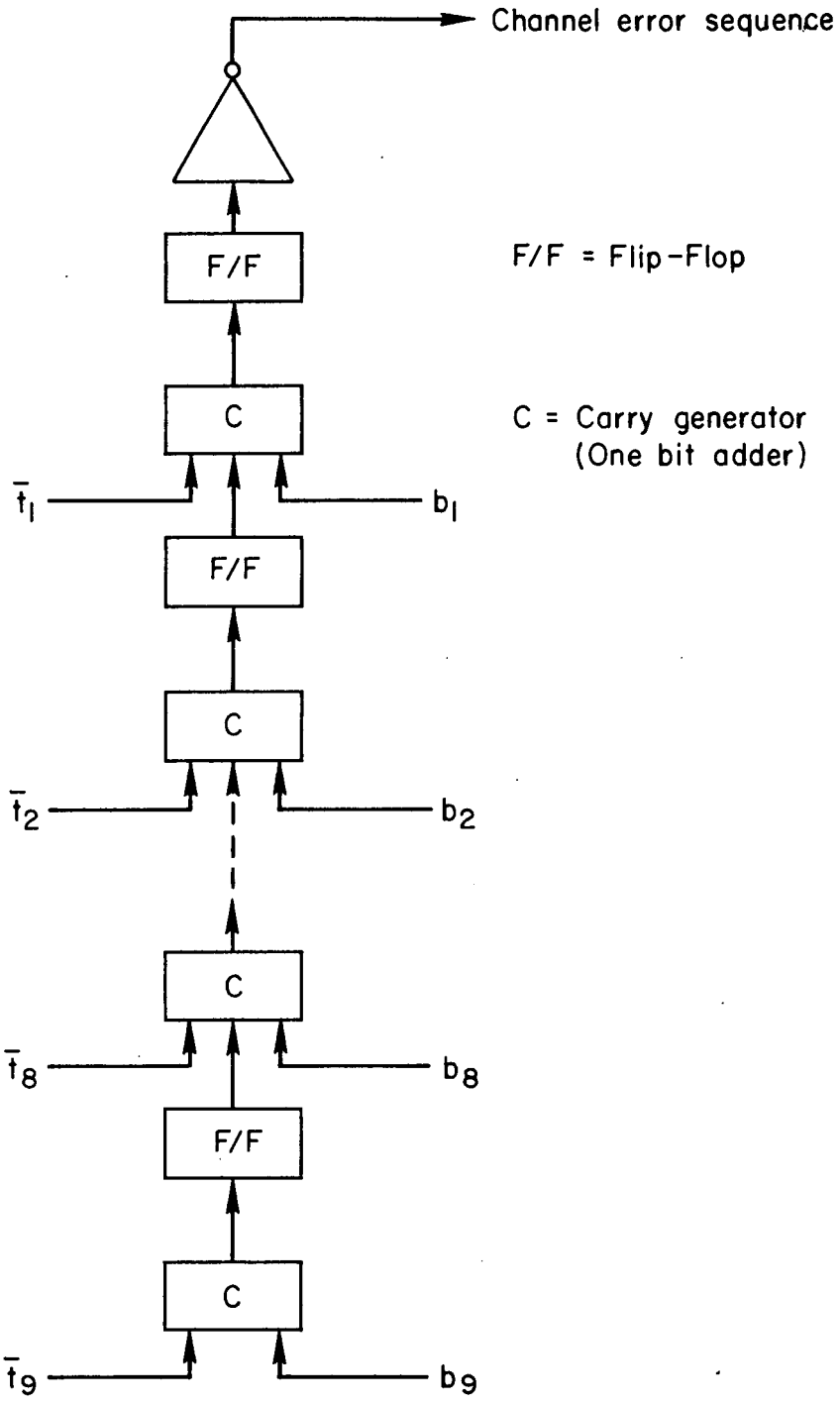


Figure I-3. "Pipeline" comparator circuit.

Notes: t_9, t_8, ... t_1 refer to the outputs from figure I-2.

b_9, b_8, ... b_1 refer to external switch settings.

APPENDIX II

SEQUENTIAL DECODING PROCESS

Sequential decoding is a procedure for systematically searching through a code tree, using received information as a guide, with the objective of eventually tracing out the path representing the actually transmitted information sequence.

The sequential decoder uses a modification of the Fano algorithm. Briefly, the operation of the Fano algorithm is as follows. Starting at the first node in the code tree, a path is traced through the tree by moving ahead one node at a time. At each node encountered, the decoder evaluates a branch metric for each branch stemming from that node. The branch metric is a function of the transition probabilities between the received symbols and the transmitted symbols along the hypothesized branch.

The decoder will initially choose the branch with the largest metric value (corresponding to the closest fit to the received symbols). The metric is then added to a path metric, which is the running sum of branch metrics along the path presently being followed. Along with the path metric, the decoder keeps track of the running threshold T. As long as the path metric keeps increasing, the decoder assumes it is on the right track and keeps moving forward, raising T to lie within a fixed constant, Δ, below the path metric. If, on the other hand, the path metric decreases at a particular node, such that it becomes less than T, the decoder assumes it may have made a mistake and backs up. It will then systematically search nodes at which the path metric is greater than T until it finds a path that starts increasing again, or until it exhausts all nodes lying above T. At this point, it is forced to lower T and search again. Eventually, it will find a path that appears to have an increasing path metric.

Eventually, the decoder will penetrate sufficiently deep into the tree, that with high probability the first few branches followed are correct, and will not be returned to by the decoder in a backward search. At this point, the information bits corresponding to these branches can be considered decoded and the decoder may erase received data pertaining to these branches.

A major problem with sequential decoding is the variability in the number of computations required per information digit decoded. The number of computations is defined as a measure of the time required to decode for a fixed decoding speed and is expressed in computations per second. The cumulative distribution of computations

performed per digit decoded, c, has been upper and lower bounded for the discrete memoryless channel by a Pareto distribution

$$Pr[c>L] \approx k\, L^{-\alpha}, \quad L>>1$$

(L represents the branch tree length)
where k is a constant and α is determined by the relationship

$$R = \frac{E_o(\alpha)}{\alpha}$$

where R is the code rate.

Here $E_o(\alpha)$ is a convex function of α which is determined by the channel transition probabilities, which are in turn a function of E_b/N_o. This function has the properties that $E_o(0) = 0$, and $E_o(1) = R_{comp}$. Therefore, we can see that if $R = R_{comp}$, $\alpha = 1$. R_{comp} is the so-called computational cutoff rate of sequential decoding.

Because $\alpha > 1$ for $R < R_{comp}$, the average number of computations per node decoded is finite, but for rates greater than R_o, this average is unbounded. Actually, for finite constraint lengths, the computation distributions drop off faster than the Pareto distribution for very large L. Thus, the average computations remain finite but large for $R > R_o$.

Because of the variability of the amount of computation required, there is a non-zero probability that incoming received data will fill up the decoder memory faster than old outgoing data can be processed. If the decoder tries to search a node for which received data has passed out of buffer memory, an overflow is said to occur. When an overflow occurs, the decoder must have some mechanism for moving forward to new data, reacquiring code synchronization and starting to decode again.

A guess and start overflow recovery technique has been implemented. When an overflow occurs, the decoder jumps ahead of new data, and guesses the coder state at that point based upon received data.

The probability of overflow for sequential decoding can be related to the distribution of computations per bit only in an approximate manner. Suppose the decoder has a speed factor of μ, that is, it is able to perform μ computations per branch

worth of data received. Suppose also, a decoder buffer capable of storing B branches worth of received data is used. With an initially empty buffer, the decoder may perform μB computations in progressing one bit deeper before an overflow occurs. Thus, the initial overflow probability is

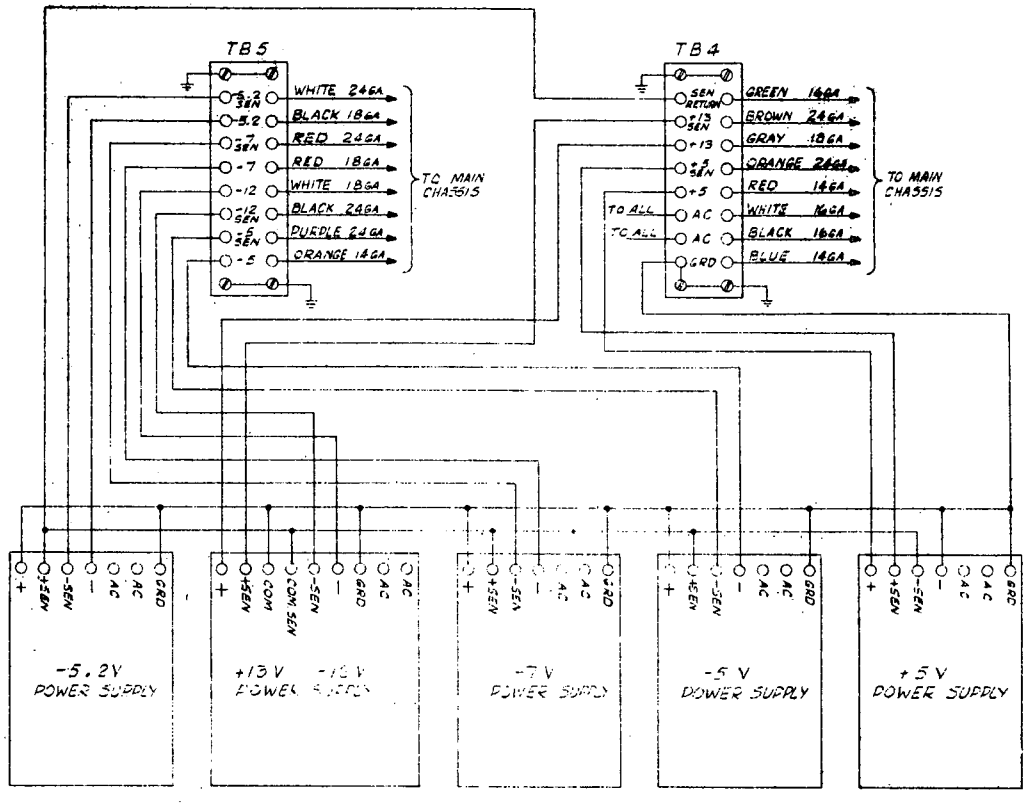
$$P_O = k\,(\mu B)^{-\alpha}$$

Since overflows can occur through the concatenation of several shorter searches, one intuitively expects that the actual overflow probability would be larger than this. However, as long as μ is somewhat larger than the average number of computations per bit, this approximation has been shown to be remarkably accurate. Of course, when an overflow does occur, many bits will be lost. Thus, the rate of bits lost due to overflow, P_{OB}, will be LP_O. One readily sees from this relationship that the composite output error rate of the system increases with each overflow. Thus, if the speed factor, μ, can be maintained as high as possible, the number of overflows will be minimized.

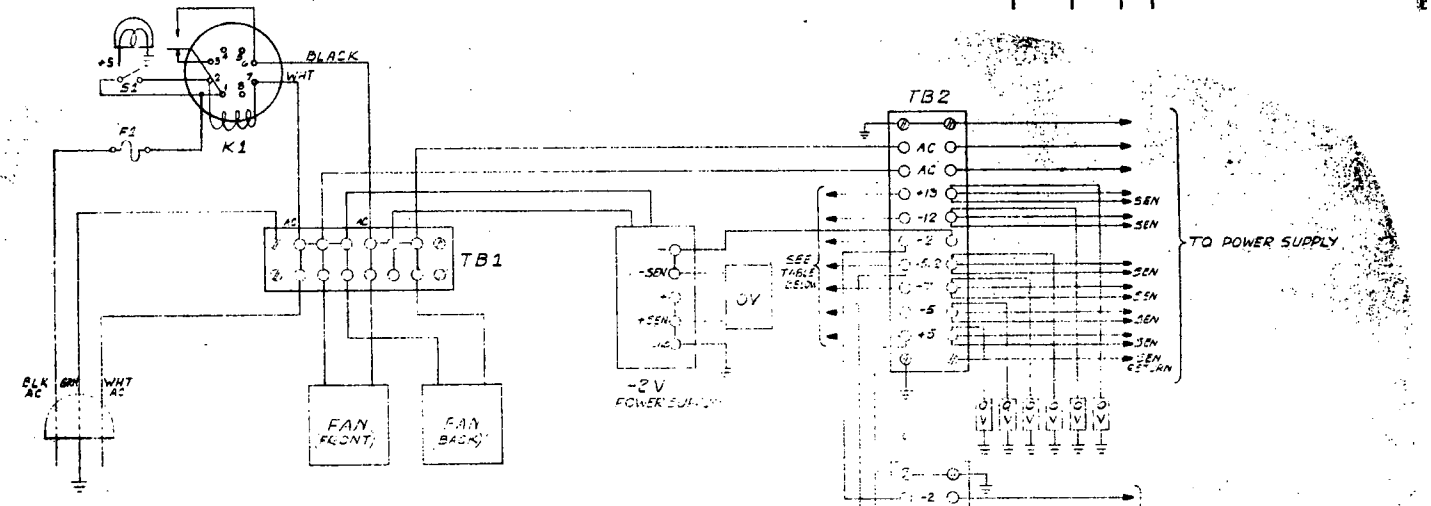
APPENDIX III - SCHEMATICS

TABLE OF CONTENTS

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



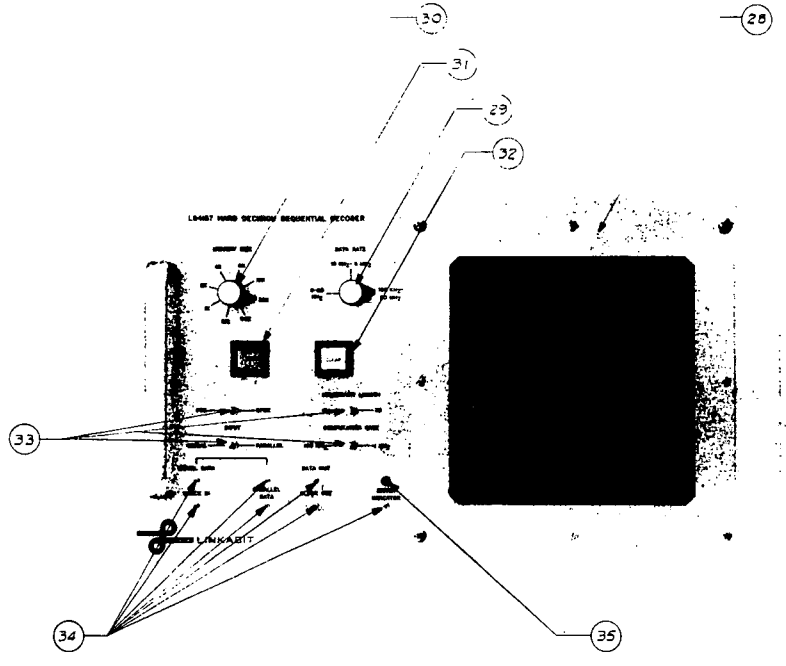
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. N/A	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX ± .XXX	DRAWN BY S. CRAYTON DATE 2/11/82	TITLE: POWER SUPPLY UNIT WIRING DIAGRAM
SURFACES ✓	CHECK	
MATERIAL	ENGINEER	
SPEC	PROJECT	
	III-1	SIZE C · CAGE IDENT NO. 11627 · DWG NO. WD 1025
		SCALE — · WEIGHT · SHEET 1 OF 1



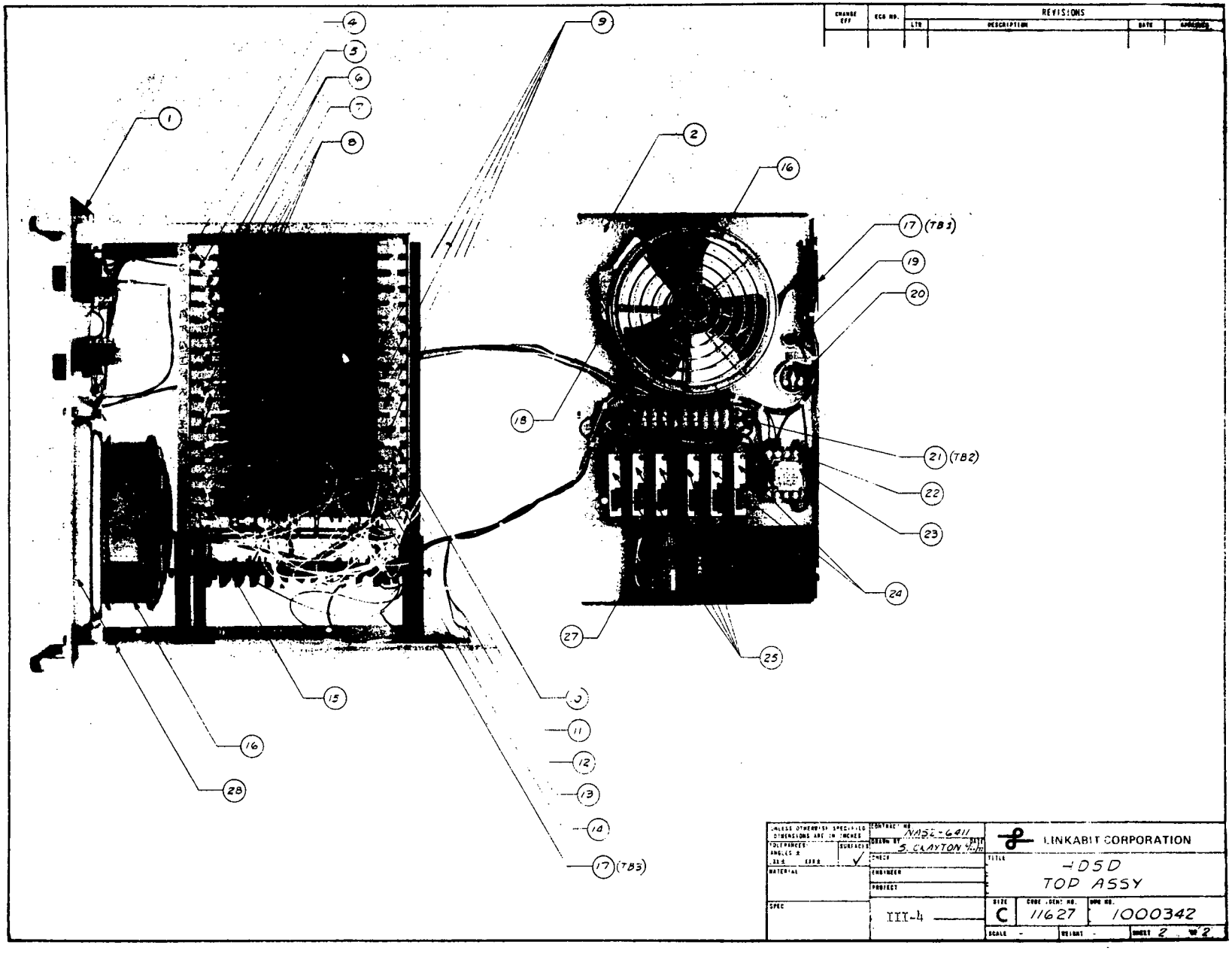
VOLTAGE	BOARD	PIN #'S
GND	A,B,S,R,S,T	1,2,25,31,[illegible]
	C,D,E,F,H,K,M,P	[illegible]
	S,J,L,N	1,2,5,17,43,49,50,[illegible]
+5.2	A	5
	C,D,E,F,H,K,M,P	[illegible]
	S,J,L,N	[illegible]
	Q	[illegible]
-5.2	A,B,S,R,S,T	3,4,25,36,55,61,[illegible]
-2.0	A,B,S,R,S,T	5,[illegible]
+12.0	R,L,N	42,[illegible]
-12.0	R,L,N	43
+15.0	C,E	7,13,[illegible],23,24,35,59,25
-5.2	C,D	9,15,[illegible],44,56,70,21,33

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. AAC 3411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX ± .XXX	DRAWN BY S. CRAYTON 7/8/75	TITLE MAIN CHASSIS POWER WIRING
SURFACES ✓	CHKD	
MATERIAL	ENGINEER	
SPEC	PROJECT TTT-2	SIZE C CODE IDENT NO. 11627 DWG NO. WD-1026
		SCALE - WEIGHT - SHEET 1 OF 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± .XX ± .XXX ± SURFACES ✓ MATERIAL SPEC	CONTRACT NO. NAS5-6411 DRAWN BY S. CRAYTON CHECK ENGINEER PROJECT III-3	LINKABIT CORPORATION TITLE HDSD TOP ASSY SIZE C · CODE IDENT NO. 11627 · DWG NO. 1000342 SCALE – · WEIGHT – · SHEET


CHANGE EFF
ECO NO.
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
16
17 (TB3)
17 (TB3)
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19
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21 (TB2)
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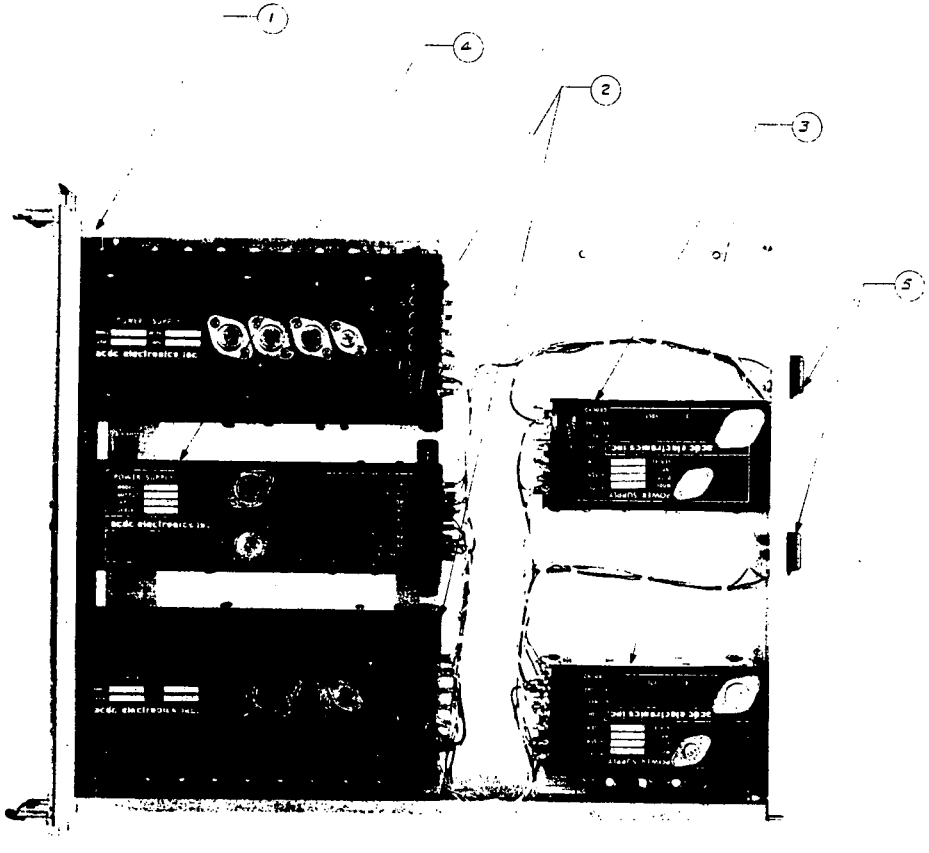
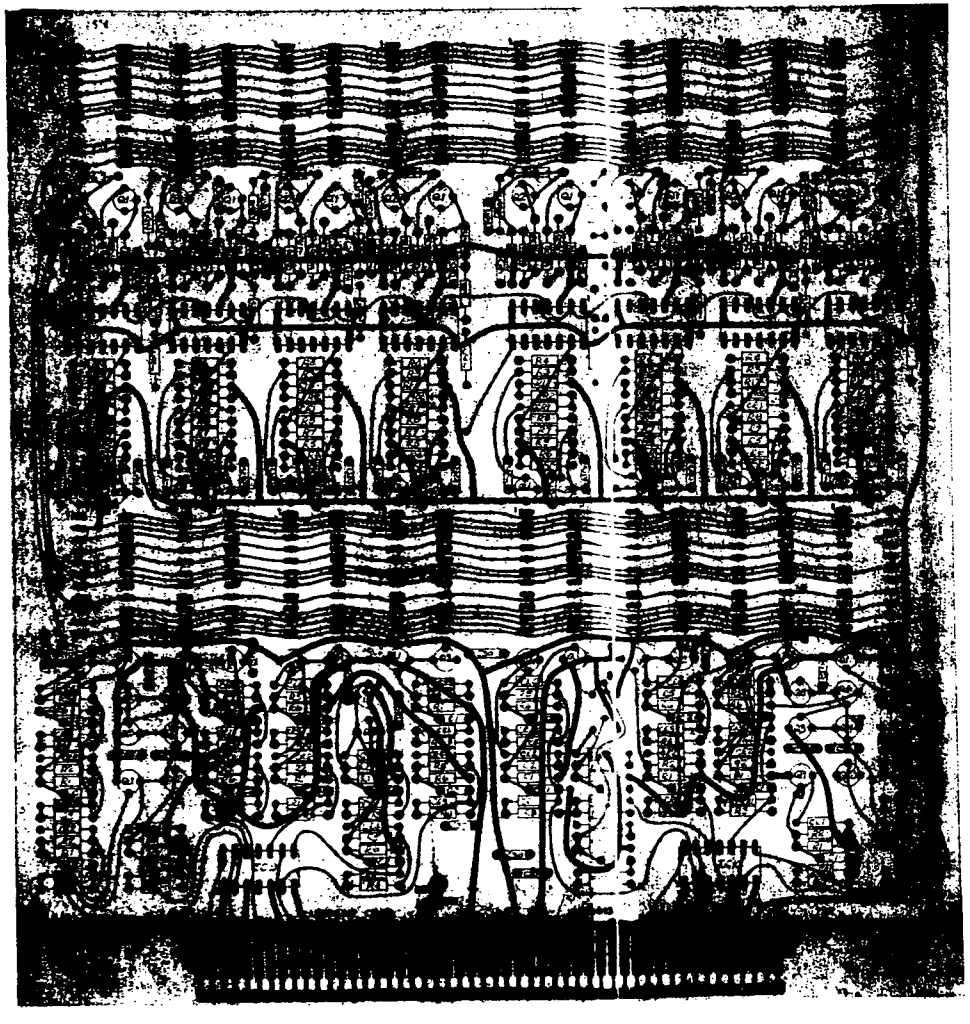
28
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±
.XX ±
.XXX ±
SURFACES
MATERIAL
SPEC
CONTRACT NO
NAS2-6411
DRAWN BY
S. CLAYTON
CHECK
ENGINEER
PROJECT
III-4
LINKABIT CORPORATION
TITLE
-D5D
TOP ASSY
SIZE
C
CODE IDENT NO.
11627
DWG NO.
1000342
SCALE
WEIGHT
SHEET 2 OF 2

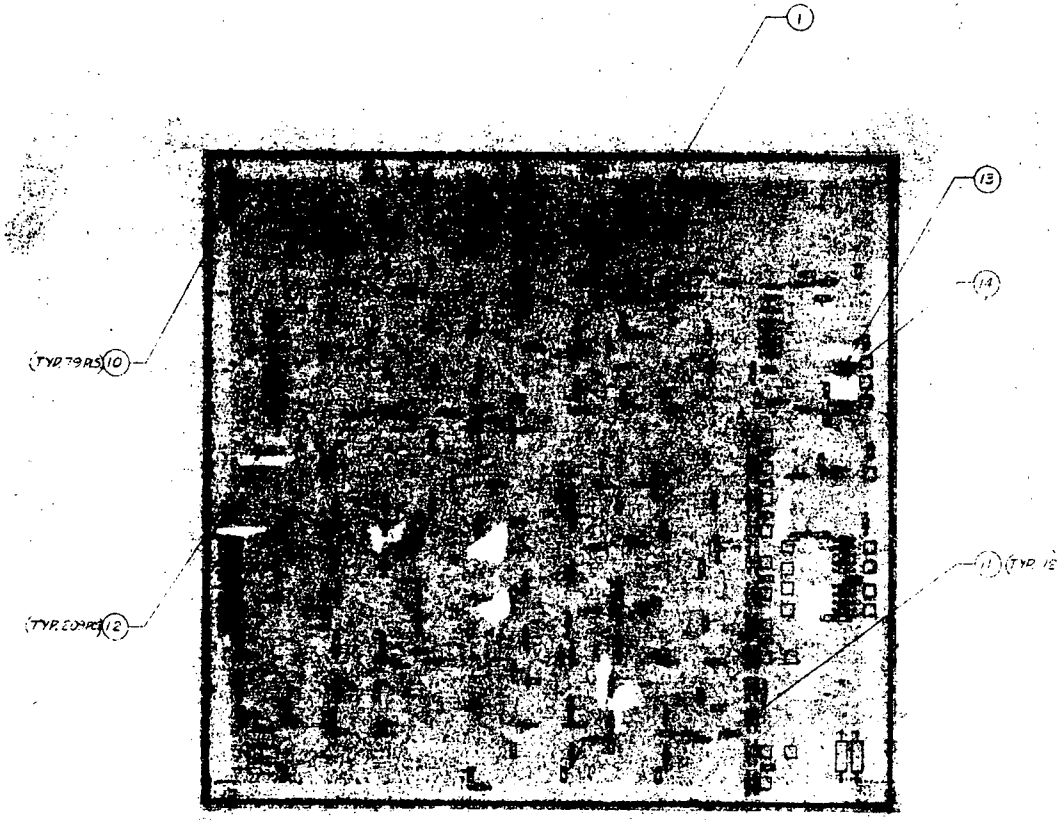
CHANGE REF	ECO NO	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY S. CRAYTON DATE
MATERIAL	CHECK	TITLE HDSD POWER SUPPLY UNIT
	ENGINEER	
SPEC	PROJECT	
	III-5	SIZE C CODE IDENT NO. 11627 DWG NO. 1000343
		SCALE - WEIGHT - SHEET 1 OF 1



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



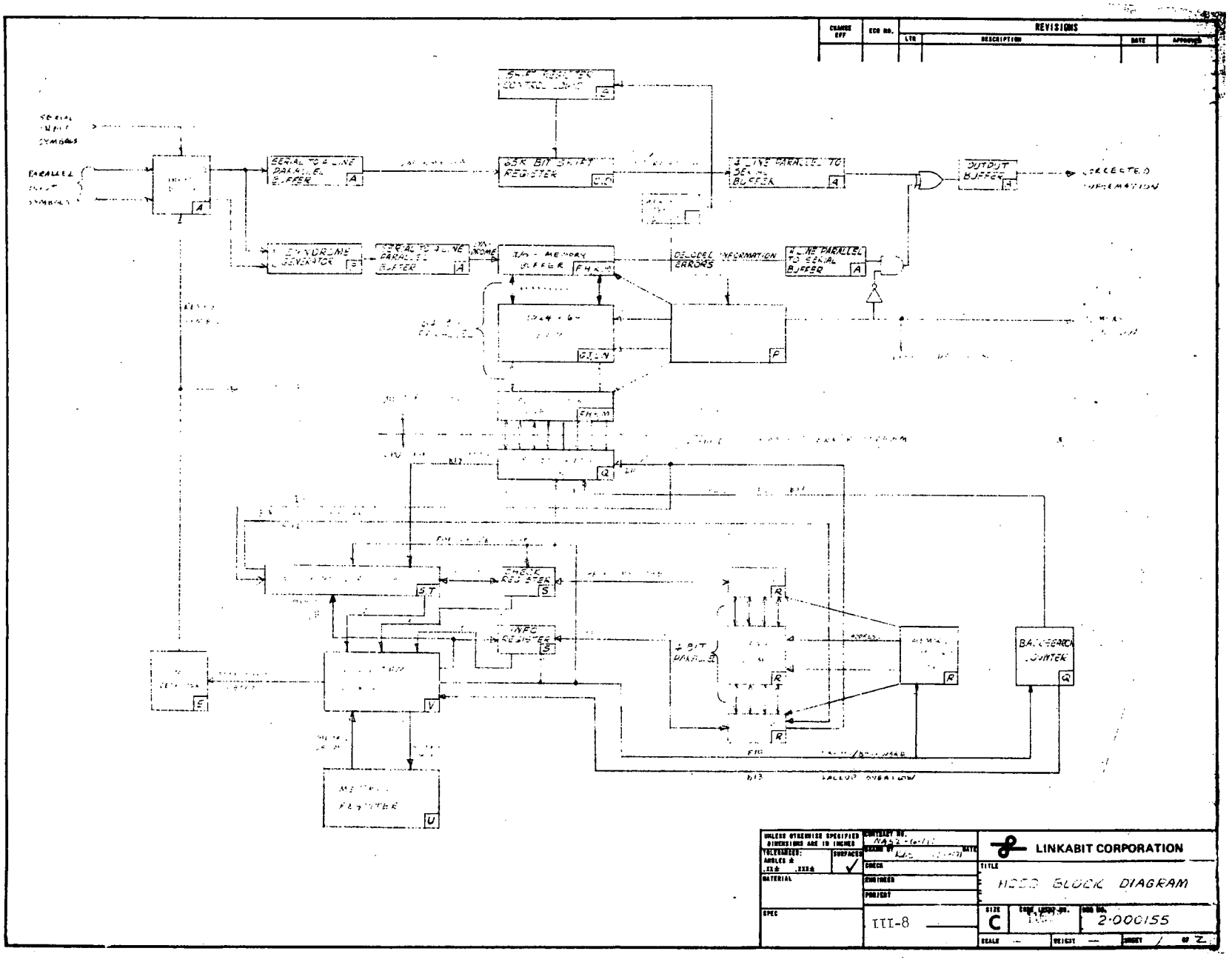
COMPONENT MOUNTING
SIDE - 1

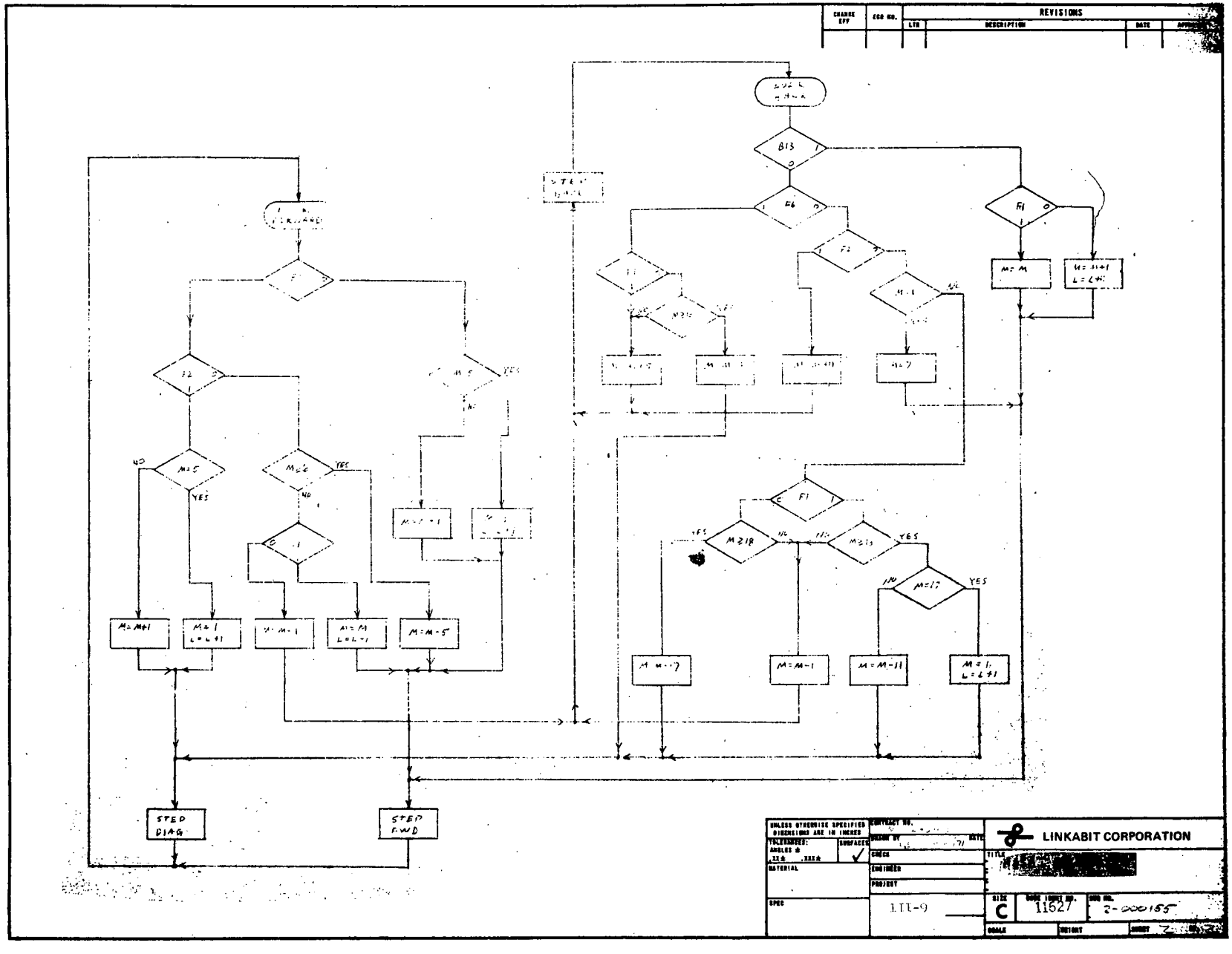
NOTES:

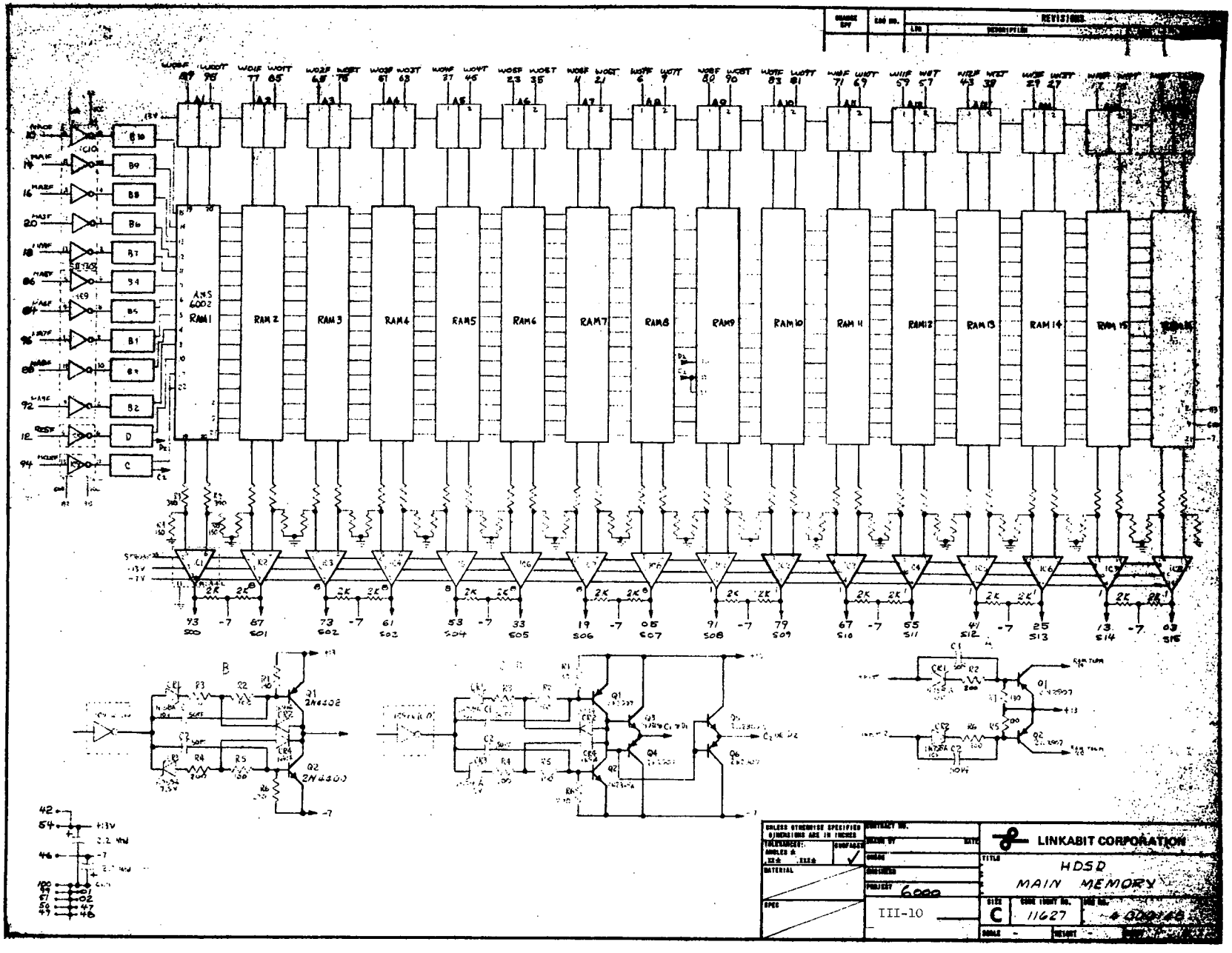
1. LOCATIONS FOR I.C. SOCKETS ON BOARD

FOR LIST OF PARTS SEE PL100018G

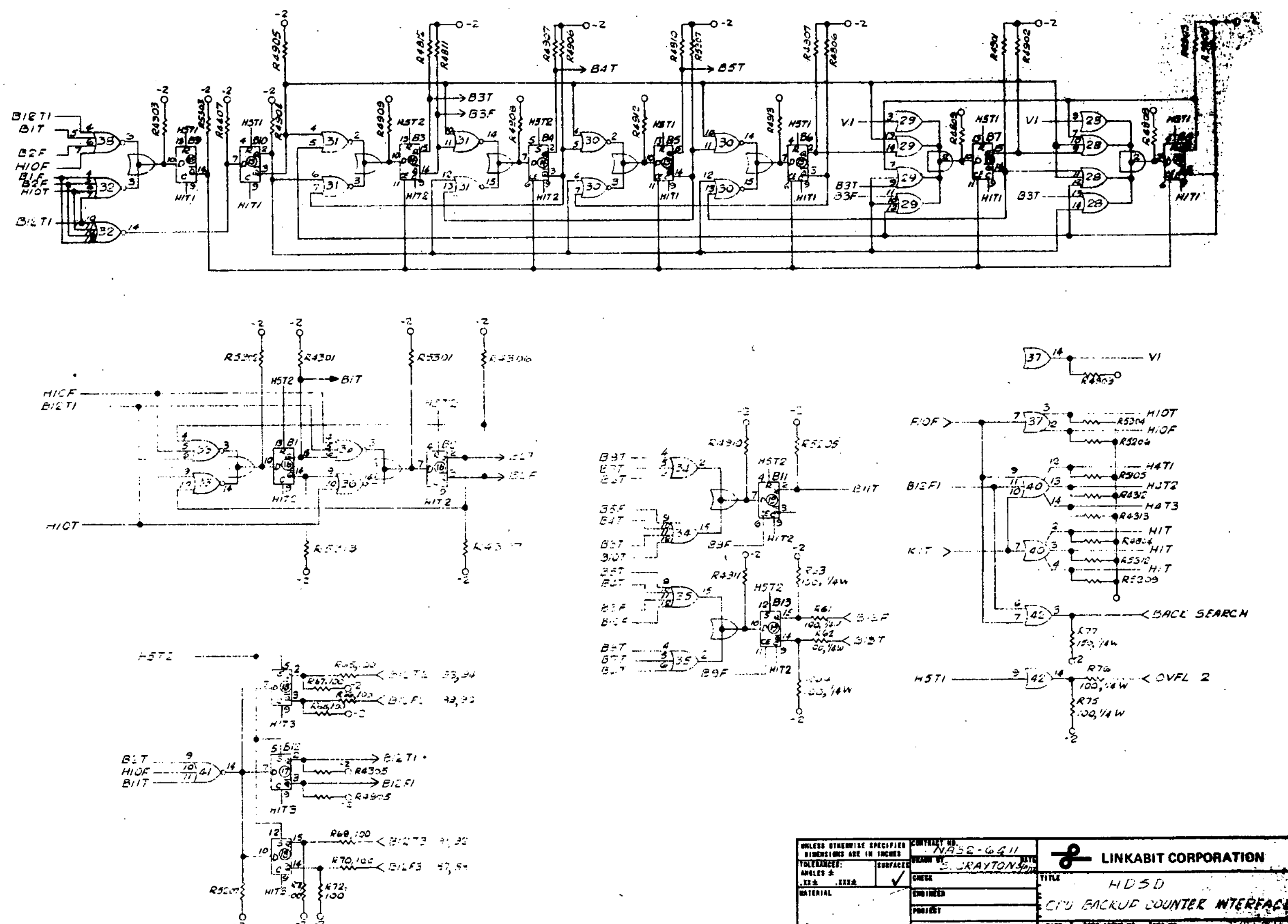
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± .XX ± .XXX ±	CONTRACT NO. NAS2-5411 DRAWN BY D. CRAYTON 4/5 CHECK ENGINEER PROJECT	LINKABIT CORPORATION TITLE: HDSD ALGORITHM LOGIC PC BOARD ASSEMBLY
MATERIAL SPEC	III-7	SIZE C · CODE IDENT NO. 11657 · DWG NO. 1000186 SCALE · WEIGHT · SHEET 1 OF 1


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
SERIAL TO 4 LINE PARALLEL BUFFER
63K BIT SHIFT REGISTER
4 LINE PARALLEL TO SERIAL BUFFER
OUTPUT BUFFER
SYNDROME GENERATOR
SERIAL TO 4 LINE PARALLEL BUFFER
I/O - MEMORY BUFFER
DECODED ERRORS
4 LINE PARALLEL TO SERIAL BUFFER
CHECK REGISTER
INFO REGISTER
4 BIT PARALLEL
BACKSEARCH COUNTER
MEMORY REGISTER
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
MATERIAL
SPEC
CONTRACT NO.
DRAWN BY
DATE
CHECK
ENGINEER
PROJECT
III-8
LINKABIT CORPORATION
TITLE
HDDD BLOCK DIAGRAM
SIZE
C
DWG. NO.
2-000155
SCALE
WEIGHT
SHEET
OF 2


REVISIONS
LTR
DESCRIPTION
DATE
B13
F6
F1
F2
M=5
M≤4
M=M+1
M=1
L=L+1
M=M-1
M=M-5
STEP DIAG
STEP FWD
M≥8
M=7
M=M
M=M-7
M=M-11
M=17
LINKABIT CORPORATION
SIZE
C
11627
III-9

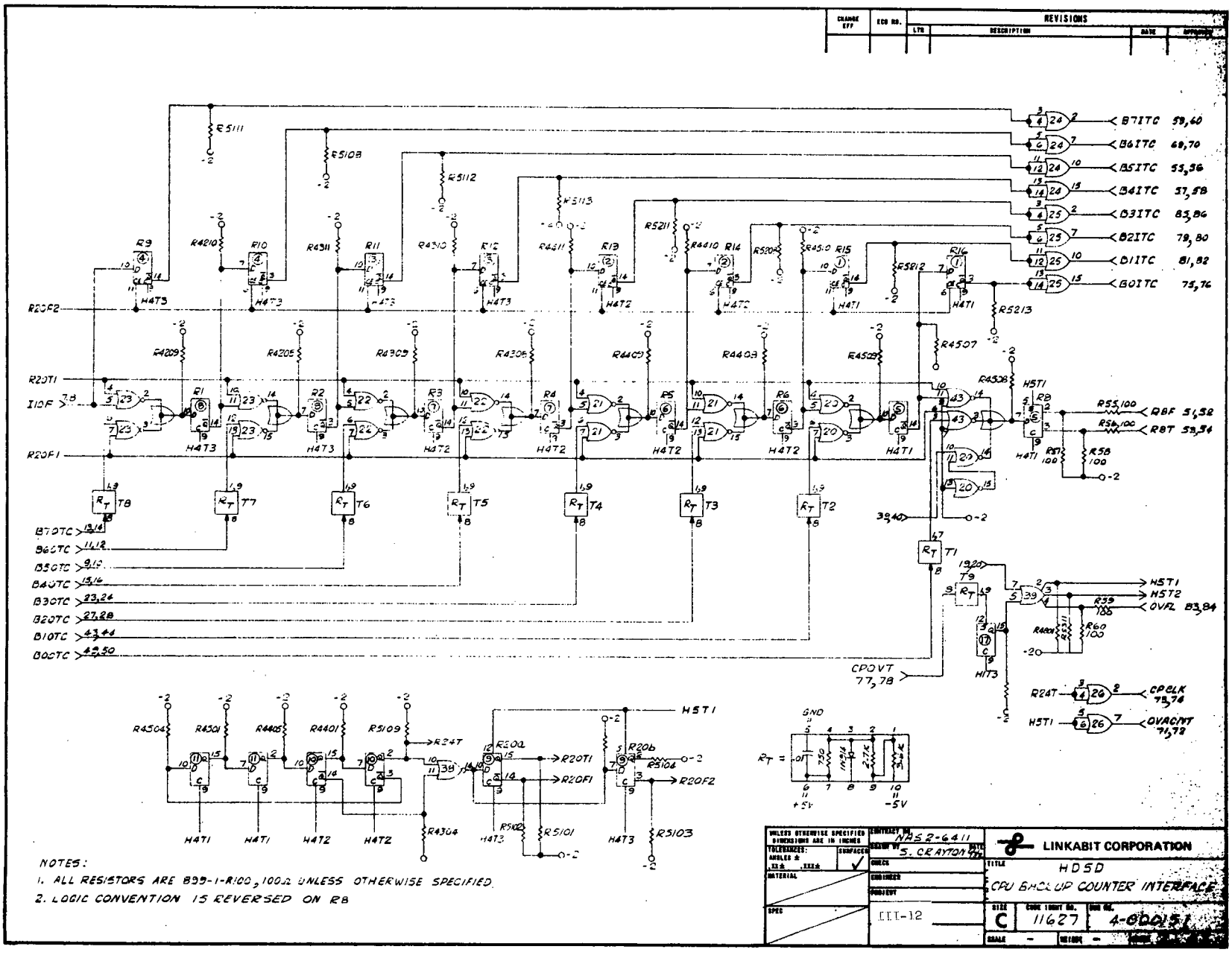

AMS 6002 RAM1
RAM 2
RAM 3
RAM 4
RAM 5
RAM 6
RAM 7
RAM 8
RAM 9
RAM 10
RAM 11
RAM 12
RAM 13
RAM 14
RAM 15
RAM 16
LINKABIT CORPORATION
HDSD
MAIN MEMORY
6000
III-10
11627

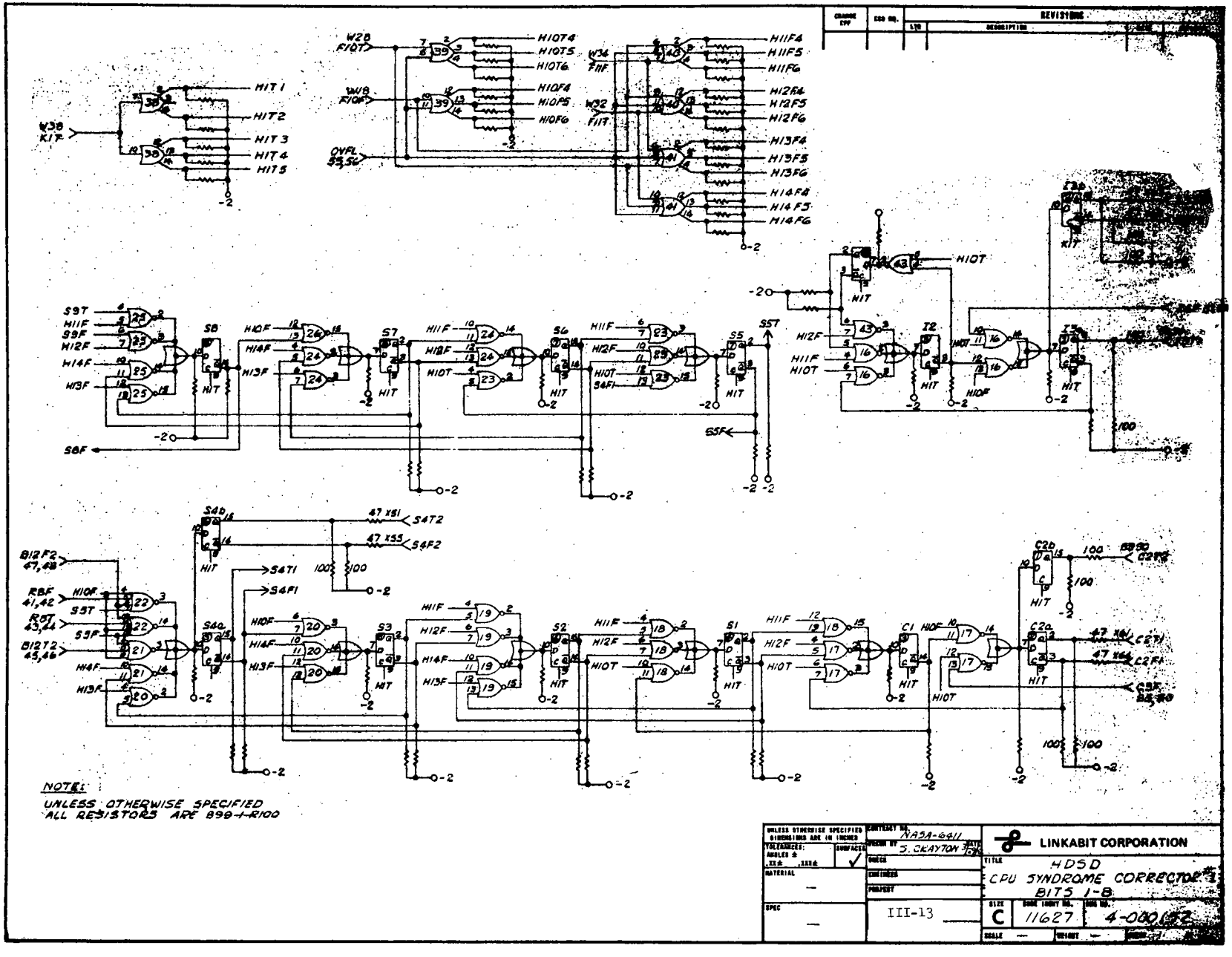
57<

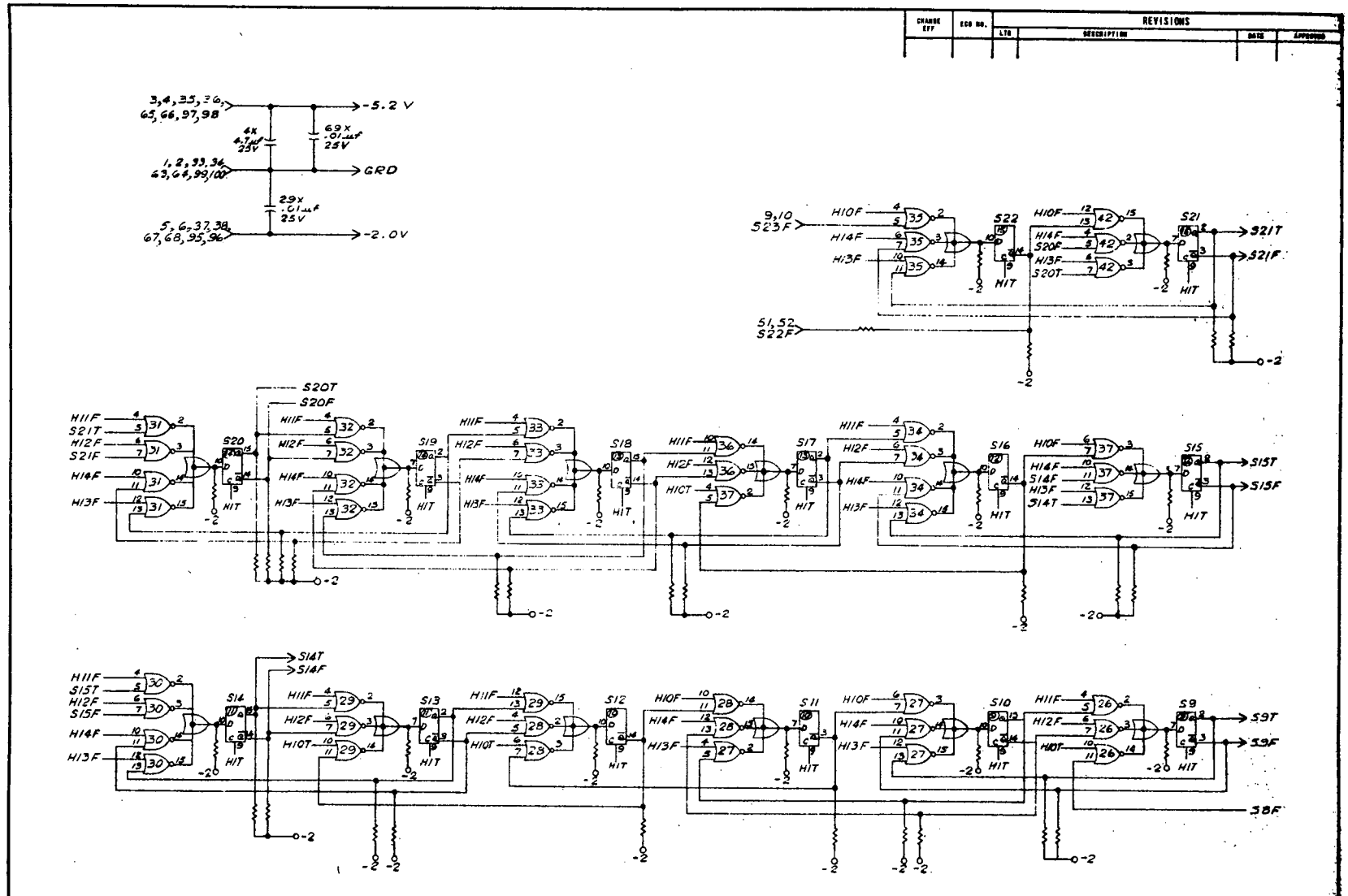


CONTRACT NO.	NAS2-6411
DRAWN BY	S. CRAYTON
	LINKABIT CORPORATION
TITLE	HDSD CPU BACKUP COUNTER INTERFACE
SIZE	C
CODE IDENT NO.	11627
DWG NO.	4-000

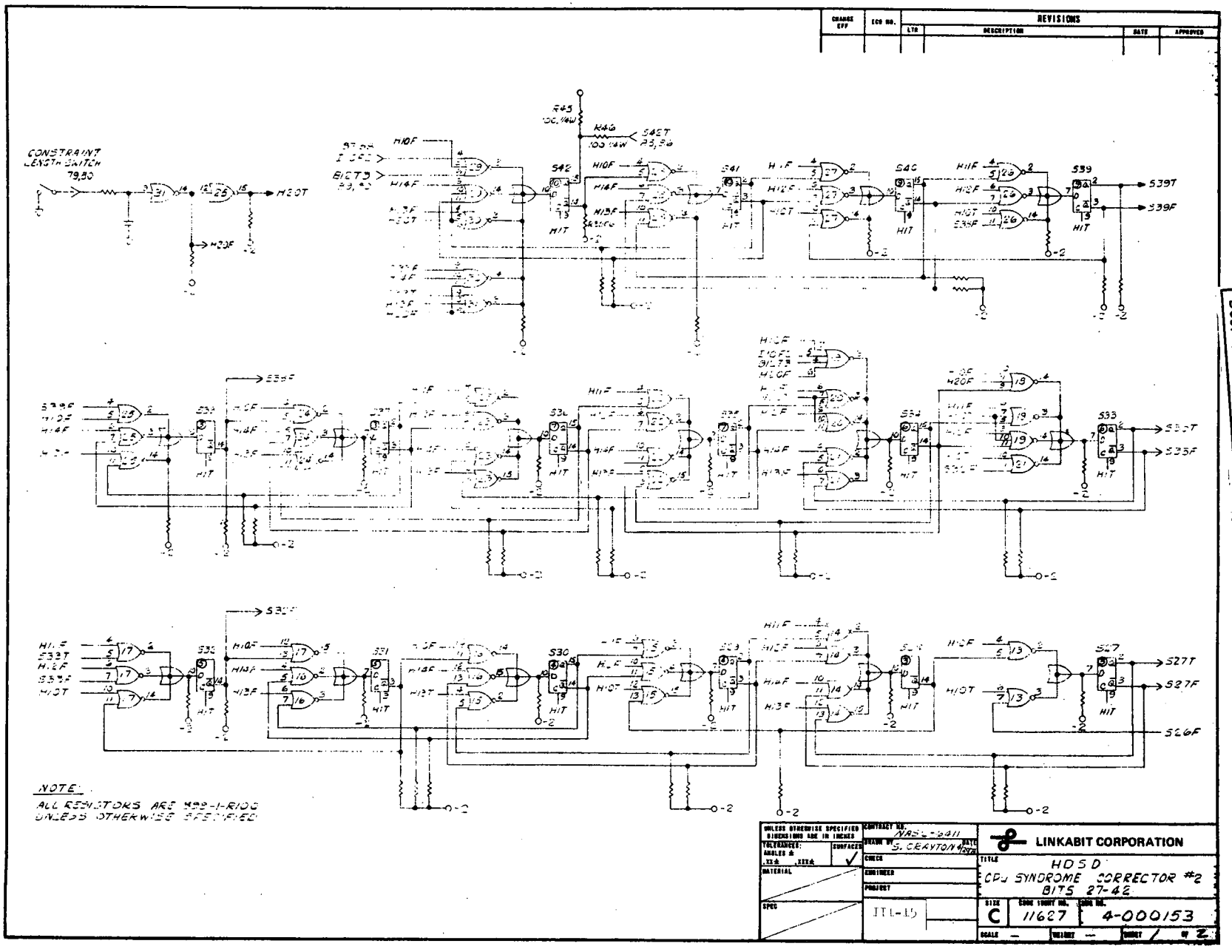
III-31

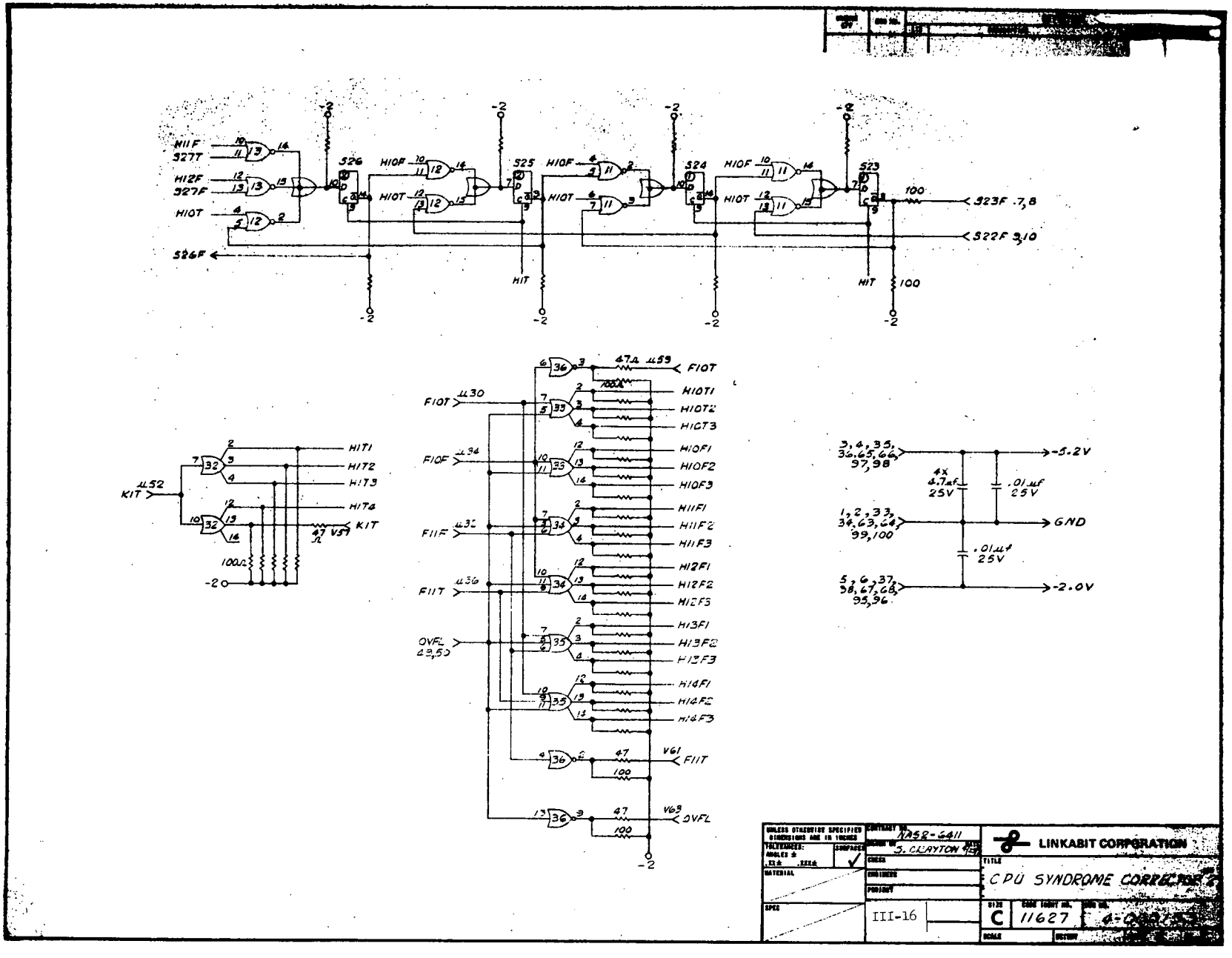

REVISIONS
LTR
DESCRIPTION
DATE
B7ITC 59,60
B6ITC 69,70
B5ITC 53,56
B4ITC 57,58
B3ITC 83,86
B2ITC 79,80
B1ITC 81,82
B0ITC 75,76
R20F2
R20T1
I10F
R20F1
B7OTC 13,14
B6OTC 11,12
B5OTC 9,10
B4OTC 15,16
B3OTC 23,24
B2OTC 27,28
B1OTC 43,44
B0OTC 42,50
RBF 51,52
RBT 53,54
39,40
CPOVT 77,78
H5T1
H5T2
OVFL 83,84
R24T
CPCLK 75,76
OVACINT 71,72
GND
+5V
-5V
R20T1
R20F1
R20F2
H5T1
NOTES:
1. ALL RESISTORS ARE B39-1-R100,100Ω UNLESS OTHERWISE SPECIFIED.
2. LOGIC CONVENTION IS REVERSED ON RB
CONTRACT NO. NAS2-6411
DRAWN BY S. CRAYTON
LINKABIT CORPORATION
TITLE HDSD
CPU BACK UP COUNTER INTERFACE
SIZE C
CODE IDENT NO. 11627
DWG NO. 4-80015
SCALE -
WEIGHT -
III-12


W38 K1T
H1T1
H1T2
H1T3
H1T4
H1T5
W28 F1QT
W18 F1QF
OVFL S3,S2
H1QT4
H1QT5
H1QT6
H1QF4
H1QF5
H1QF6
W34 F11F
W32 F11T
H11F4
H11F5
H11F6
H12F4
H12F5
H12F6
H13F4
H13F5
H13F6
H14F4
H14F5
H14F6
S9T
H11F
S9F
H12F
H14F
H13F
S8
H10F
H14F
H13F
S7
H11F
H12F
H10T
S6
H11F
H12F
H10T
S4F1
S5
S5T
S5F
H10T
H12F
H11F
H10T
T2
H10F
T3
K1T
100
S8F
S4D
47 X51
47 X55
S4T2
S4F2
S4T1
S4F1
B12F2 47,48
RBF 41,42
RBT 43,44
B12T2 45,46
S4C
S3
S2
S1
C1
H10F
C2D
C2C
C2B
C2A
47 X61
47 X64
C2T1
C2F1
C2F2
C2T2
NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 890+-R100
CONTRACT NO. NASA-6411
DRAWN BY S. CRAYTON
LINKABIT CORPORATION
TITLE HDSD CPU SYNDROME CORRECTOR BITS 1-8
SIZE C
11627
4-000162
III-13



CONTRACT NO.	NAS2-6411
DRAWN BY	S. CRAYTON
CHECK	
ENGINEER	
PROJECT	
MATERIAL	—
SPEC	—
	III-14
	LINKABIT CORPORATION
TITLE	HDSD CPU SYNDROME CORRECTOR #2 BITS 9-26
SIZE	C
DRAWING NO.	4-000152
SCALE	—
WEIGHT	—





UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± .XX ± .XXX ± MATERIAL FINISH SIZE	CONTRACT NO. NASA-6411 DESIGNED S. CLAYTON 9/67 CHECKED ENGINEER PROJECT III-16	LINKABIT CORPORATION TITLE CPU SYNDROME CORRECTOR 2 SIZE C CODE IDENT NO. 11627 DWG NO. 4-000275 SCALE SHEET

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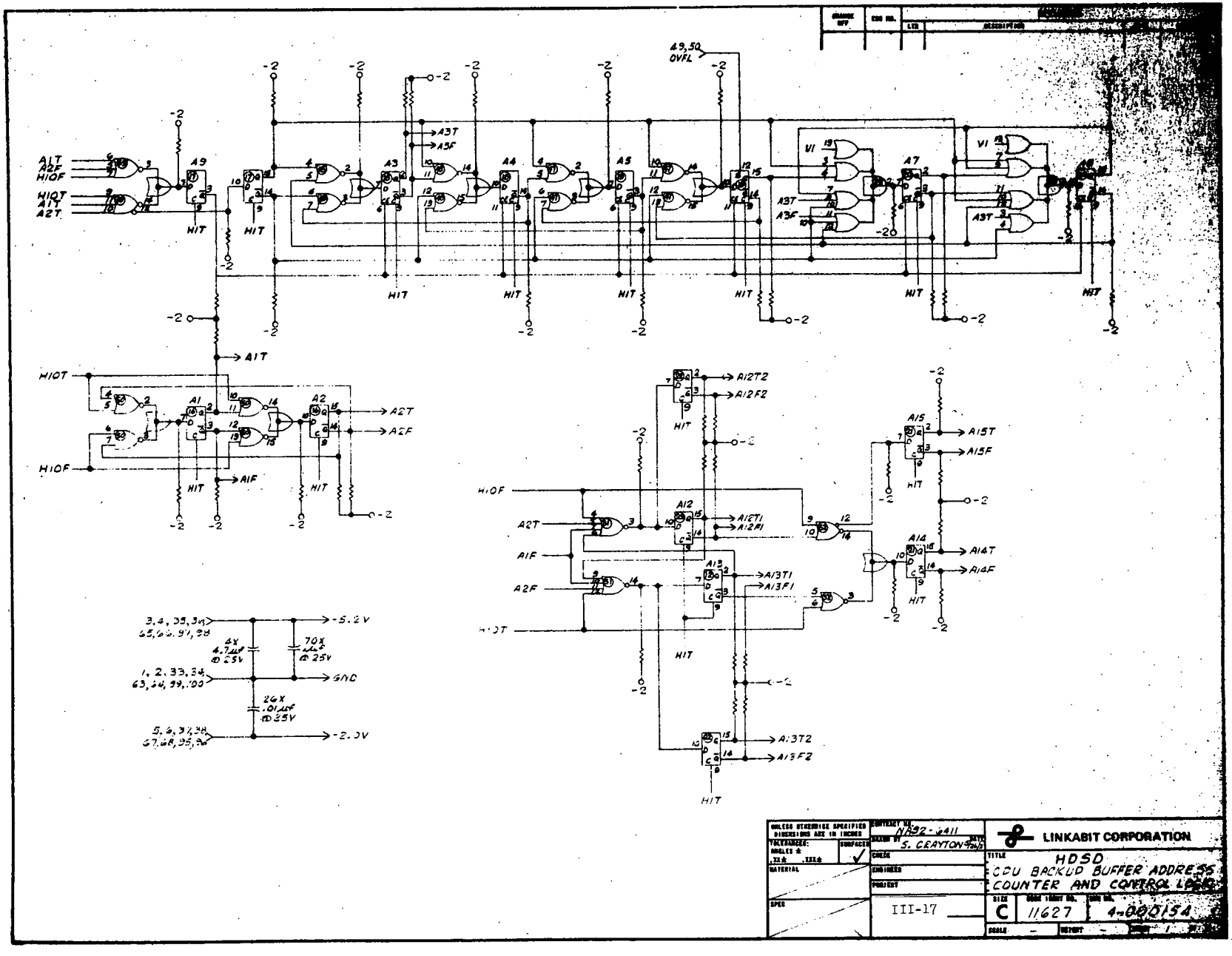
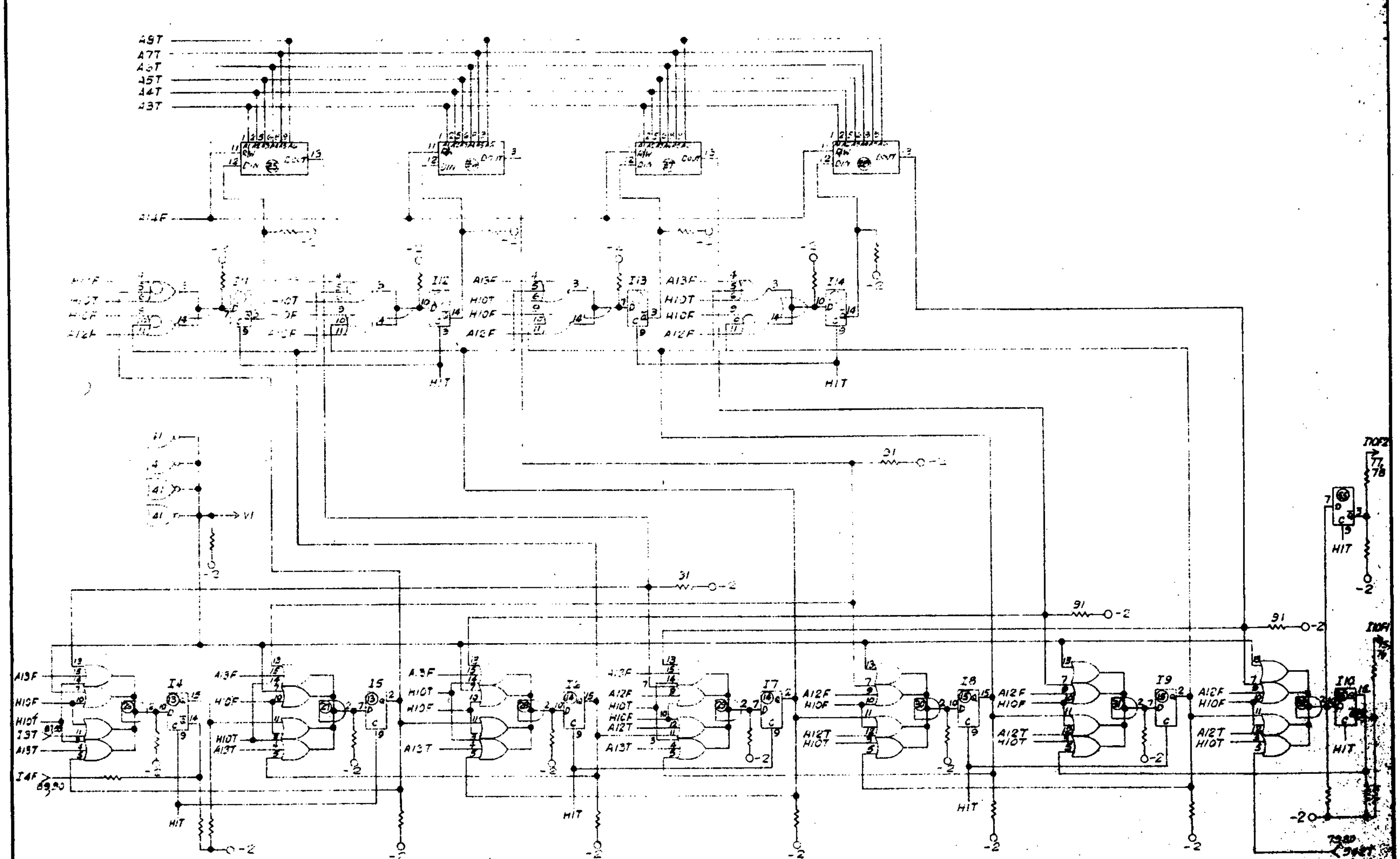
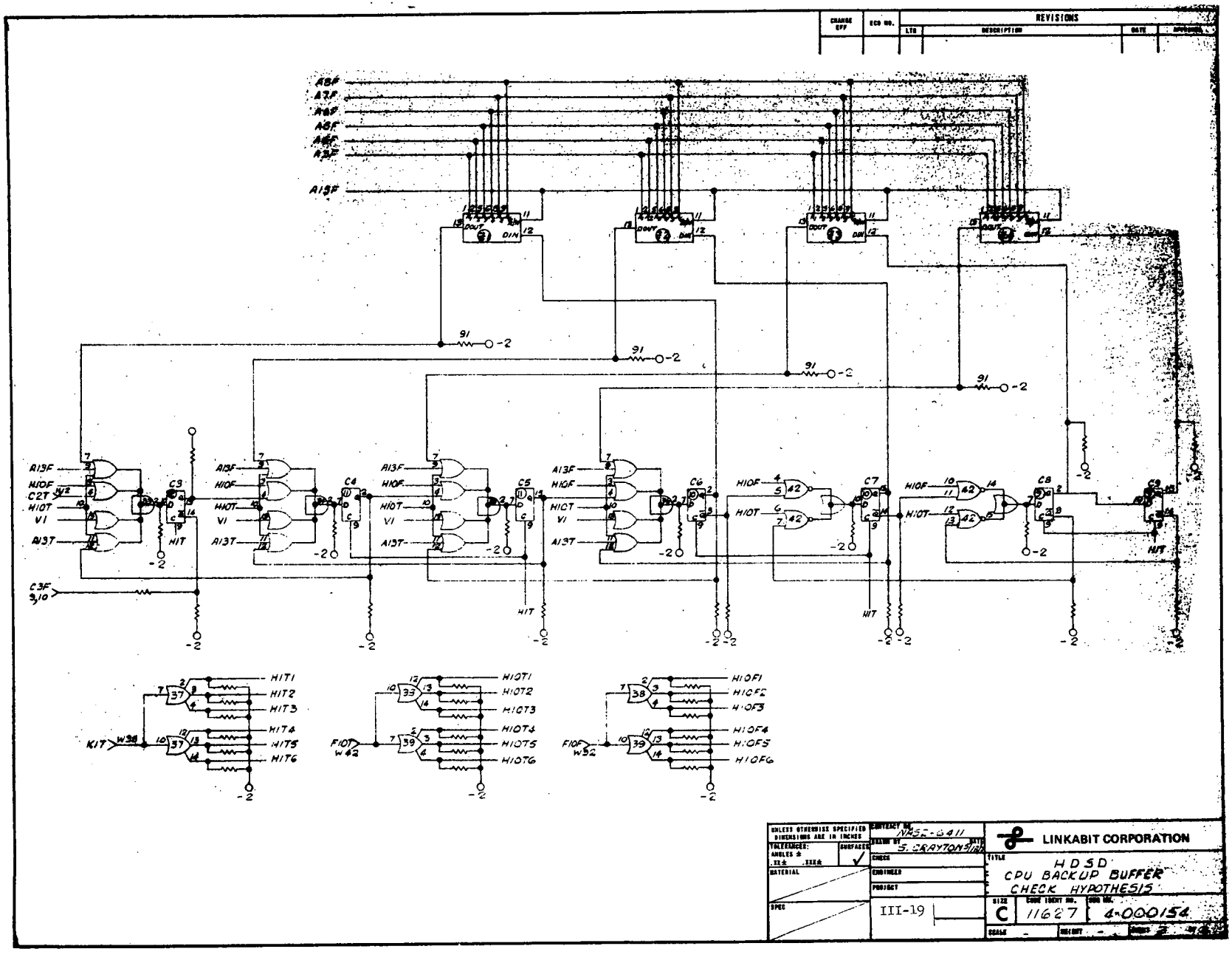
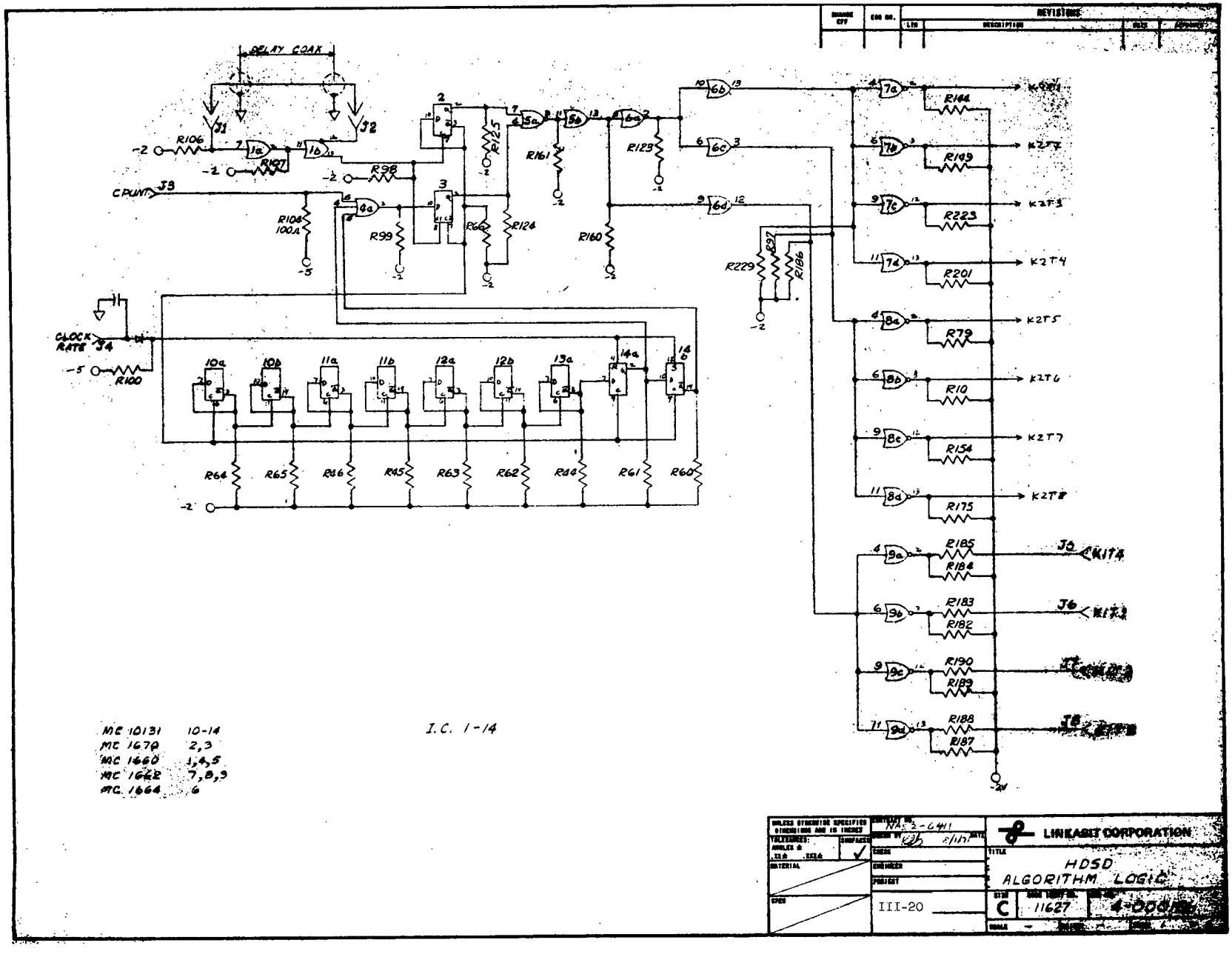

49,50 OVFL
A1T
A2F
H1OF
H1OT
A1T
A2T
HIT
A3T
A3F
A1
A2
A3
A4
A5
A7
A9
V1
A1F
A2T
A2F
H1OF
H1OT
A12T2
A12F2
A1ET1
A12F1
A13T1
A13F1
A13T2
A13F2
A15
A14
A15T
A15F
A14T
A14F
3,4,33,34,65,66,97,98
1,2,33,34,63,64,99,100
5,6,37,38,67,68,95,96
4X 4.7μF @25V
70X μF @25V
26X .01μF @25V
-5.2V
GND
-2.0V
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
.XX ± .XXX ±
SURFACES
MATERIAL
SPEC
CONTRACT NO. NA82-4411
DRAWN W. S. CRAYTON 9/6/81
CHKD
ENGINEER
PROJECT
III-17
LINKABIT CORPORATION
TITLE HDSD CDU BACKUP BUFFER ADDRESS COUNTER AND CONTROL LOGIC
SIZE C
CODE IDENT NO. 11627
DWG NO. 4-000154
SCALE –
WEIGHT –
SHEET 1



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY S. CRAYTON	TITLE HDSD CPU BACKUP BUFFER INFORMATION HYPOTHESIS
MATERIAL	CHECK / ENGINEER / PROJECT	SIZE C — CODE IDENT NO. 11627 — DWG NO. 4-[illegible]
SPEC		SCALE —

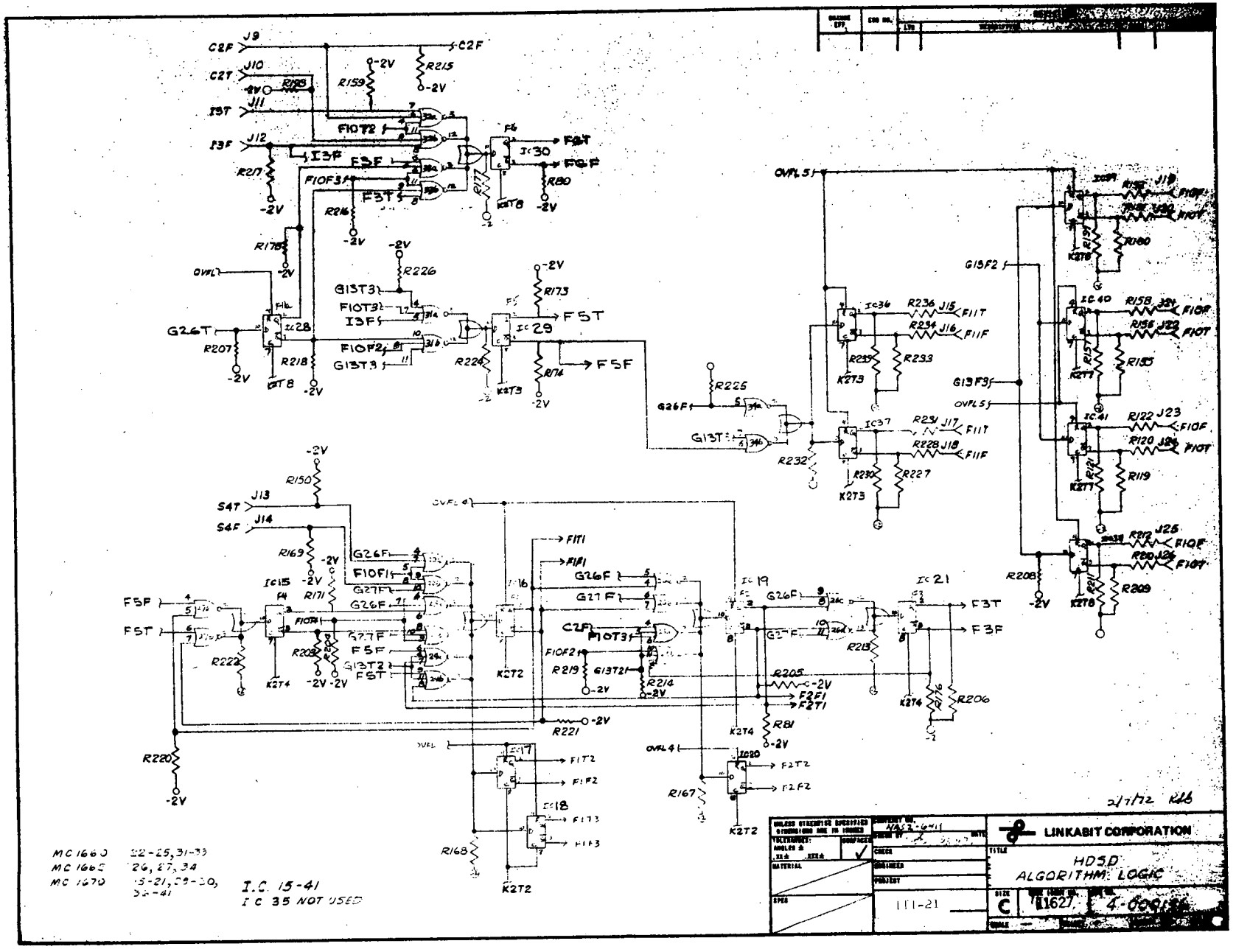

REVISIONS
A13F
A12F
A11F
A10F
A09F
A08F
A13F
91
-2
C3
C4
C5
C6
C7
C8
C9
HIT
C2T
VI
A13T
A10F
A09T
C3F
9,10
HIOF
HIOT
42
HIT1
HIT2
HIT3
HIT4
HIT5
HIT6
KIT
W38
37
HIOT1
HIOT2
HIOT3
HIOT4
HIOT5
HIOT6
FIOT
W42
39
HIOF1
HIOF2
HIOF3
HIOF4
HIOF5
HIOF6
FIOF
W32
38
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES ±
.XX± .XXX±
SURFACES
MATERIAL
SPEC
CONTRACT NO. NAS2-6411
DRAWN BY S. CRAYTON 5/12
CHECK
ENGINEER
PROJECT
III-19
LINKABIT CORPORATION
TITLE
HDSD
CPU BACKUP BUFFER
CHECK HYPOTHESIS
SIZE C
CODE IDENT NO. 11627
DWG NO. 4-000154
SCALE -
SHEET 2 OF 2



ME 10131	10-14
MC 1670	2,3
MC 1660	1,4,5
MC 1662	7,8,9
MC 1664	6

I.C. 1-14

		LINKABIT CORPORATION	
		TITLE: HDSD ALGORITHM LOGIC	
	III-20	C	11627


C2F
C2T
I3T
I3F
J9
J10
J11
J12
R215
R159
-2V
F10T2
I3F
F3F
F3T
IC30
F4
R217
R80
R216
R227
R178
OVFL
G26T
R207
R218
IC28
F1b
R226
G13T3
F10T3
I3F
F10F2
G13T3
IC29
F5
R173
F5T
R224
R74
F5F
R225
G26F
G13T
R232
IC37
R231
J17
F11T
R228
J18
F11F
R230
R227
K273
OVFL 5
IC39
R156
J19
F10T
R160
R159
K278
G13F2
IC40
R158
J21
F10F
R157
J22
F10T
R155
K277
G13F3
OVFL 5
IC41
R122
J23
F10F
R120
J24
F10T
R121
R119
K277
R208
R209
J25
R210
J26
F10F
R211
F10T
K278
-2V
R150
J13
S4T
J14
S4F
R169
R171
G26F
F10F1
G27F
IC15
F4
F10T1
G27F
G26F
F5F
F5T
R222
R208
G13T2
FST
K274
-2V -2V
OVFL 4
FIT1
FIF1
G26F
G27F
C2F
F10T3
F10F2
R219
G13T2
-2V
R214
-2V
K272
R221
-2V
R220
-2V
IC19
G26F
G27F
R205
-2V
F2F1
F2T1
R81
-2V
K274
IC21
F3T
F3F
R213
R206
K274
OVFL 4
IC20
F2T2
F2F2
R167
K272
OVFL
IC17
F1T2
F1F2
IC18
F1T3
F1F3
R168
K272
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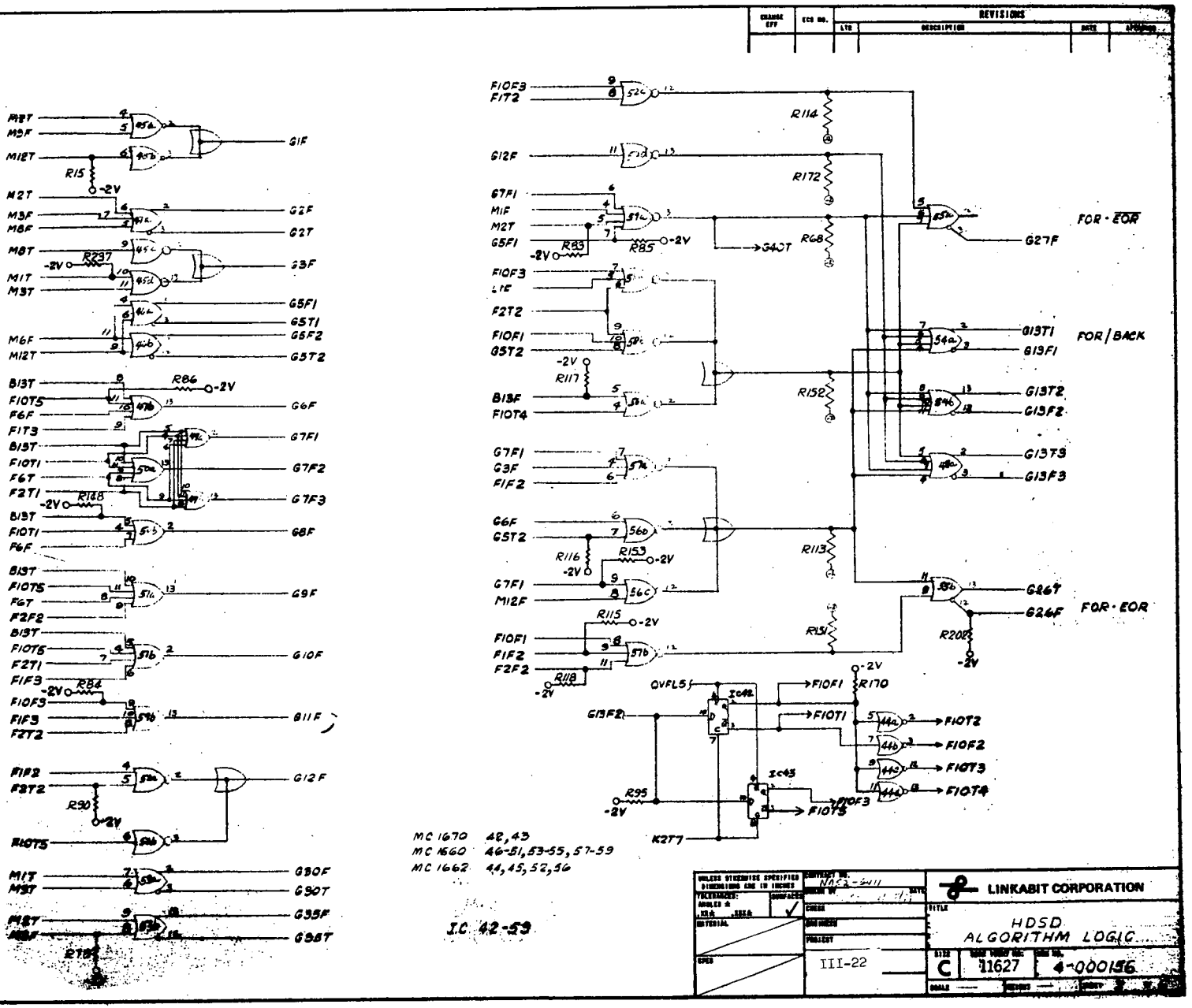
MC 1662 26, 27, 34
MC 1670 15-21, 29-30, 35-41
I.C. 15-41
I C 35 NOT USED
2/7/72 KLB
LINKABIT CORPORATION
HDSD
ALGORITHM: LOGIC
SIZE C
111-21


REVISIONS
M8T
M9F
M12T
R15
-2V
G1F
M2T
M3F
M8F
G2F
G2T
M8T
R237
G3F
M11
M13T
G5F1
G5T1
M6F
M12T
G5F2
G5T2
B13T
R86
F10T5
F6F
G6F
F1T3
B13T
G7F1
F10T1
F6T
G7F2
F2T1
R188
G7F3
B13T
F10T1
F6F
G8F
B13T
F10T5
F6T
G9F
F2F2
B13T
F10T5
F2T1
G10F
F1F3
R84
F10F3
F1F3
F2T2
B11F
F1F2
F2T2
R90
G12F
F10T5
M11
G80F
M9T
G90T
M8T
G95F
M8F
G98T
F10F3
F1T2
R114
G12F
R172
G7F1
M1F
M2T
G5F1
R83
R85
-2V
G40T
R68
FOR · EOR
G27F
F10F3
L1E
F2T2
F10F1
G5T2
G13T1
FOR/BACK
G13F1
-2V
R117
B13F
F10T4
R152
G13T2
G13F2
G13T3
G13F3
G7F1
G3F
F1F2
G6F
G5T2
R116
R153
G7F1
M12F
R113
G26T
G26F
FOR · EOR
R115
F10F1
F1F2
F2F2
R118
R151
R202
QVFL5
IC42
F10F1
R170
G13F2
F10T1
F10T2
F10F2
F10T3
F10T4
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F10T5
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MC 1662 44,45,52,56
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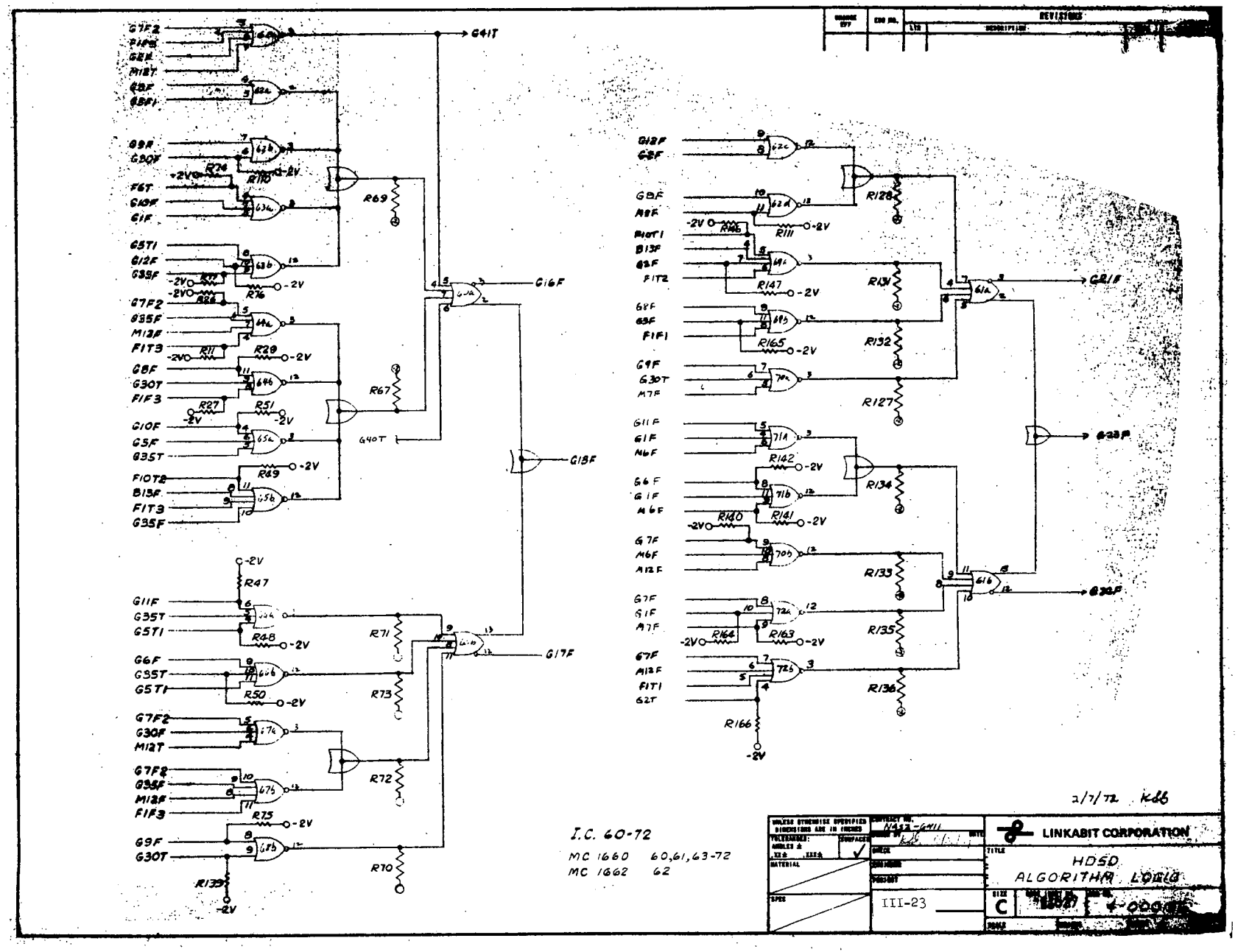
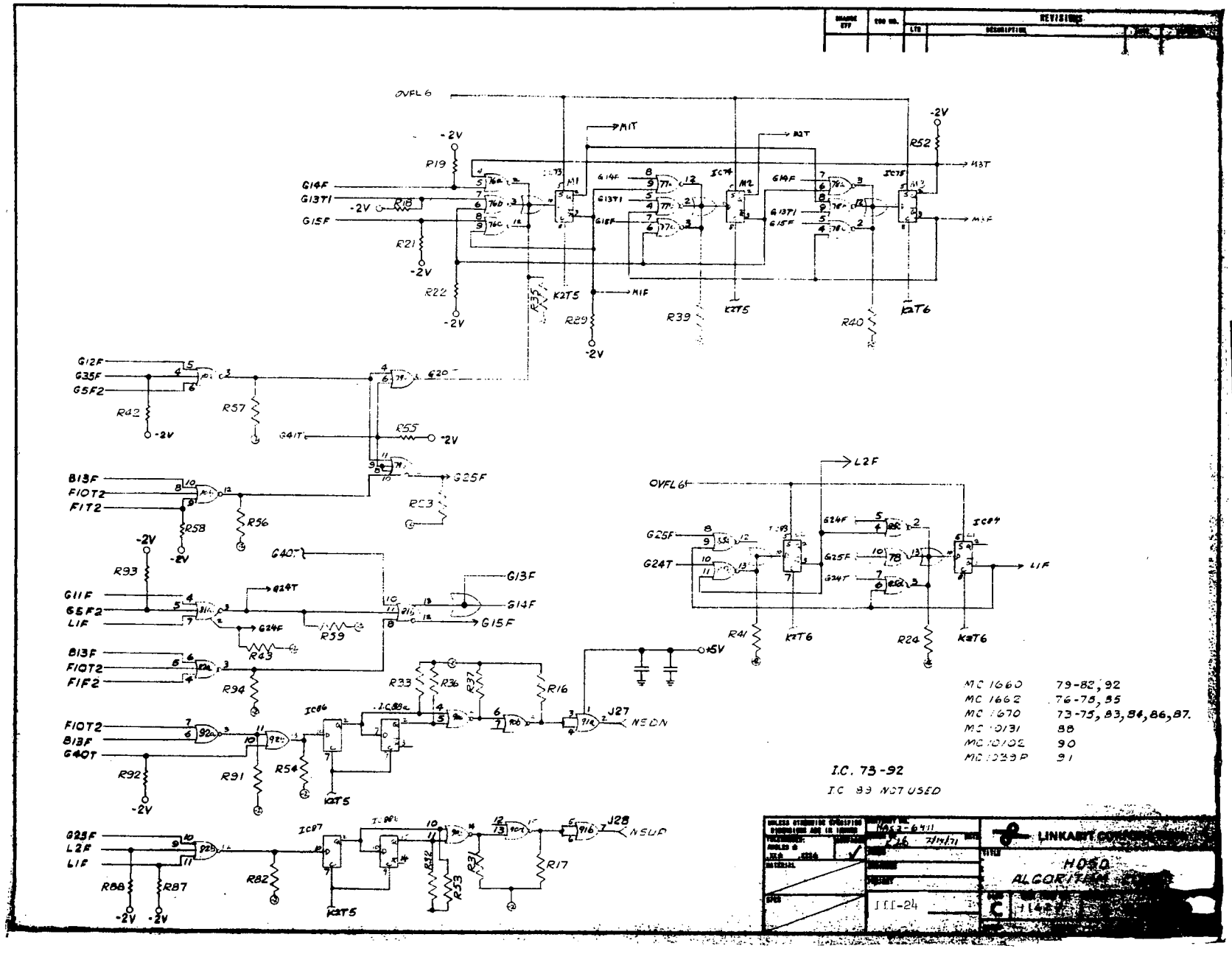
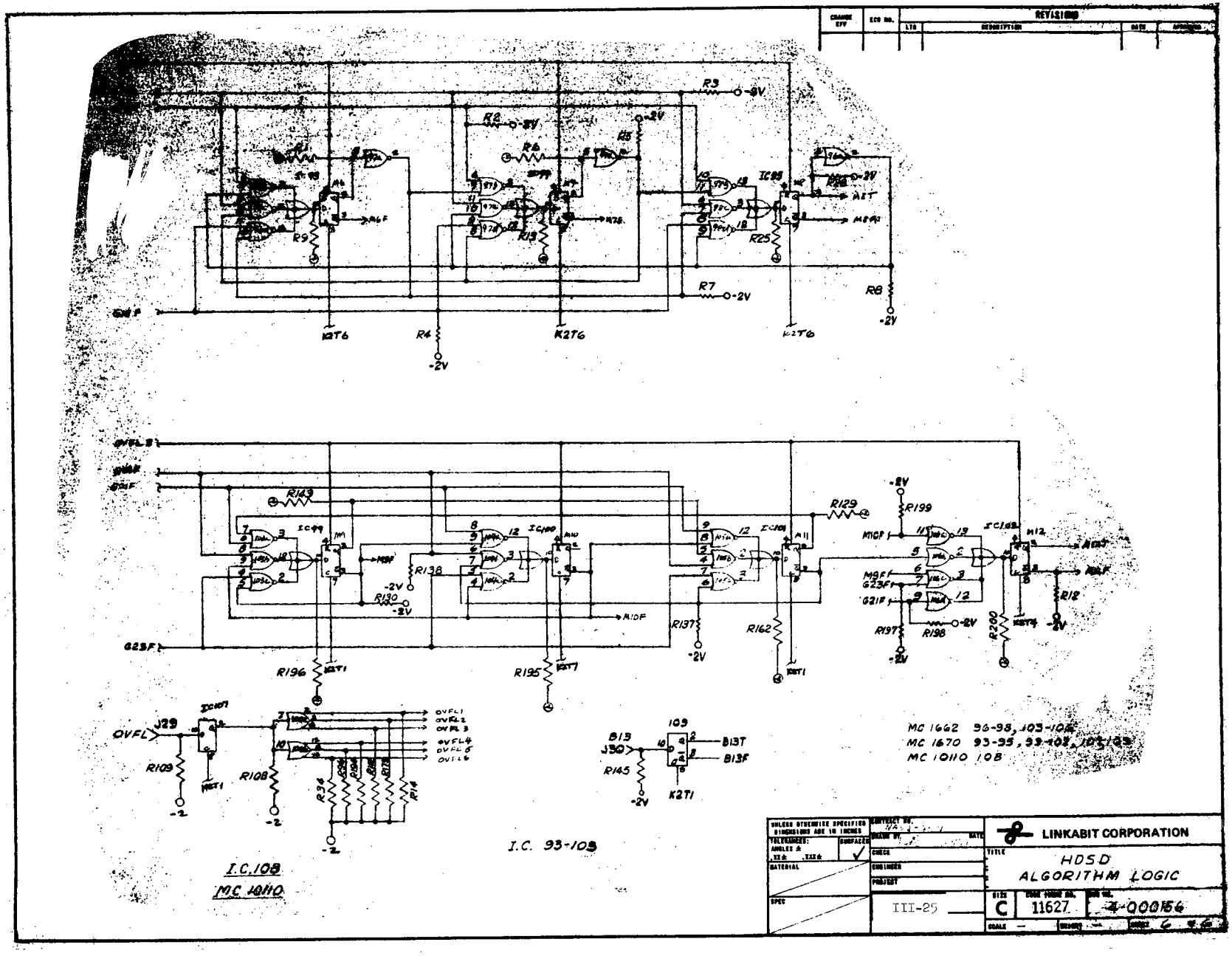
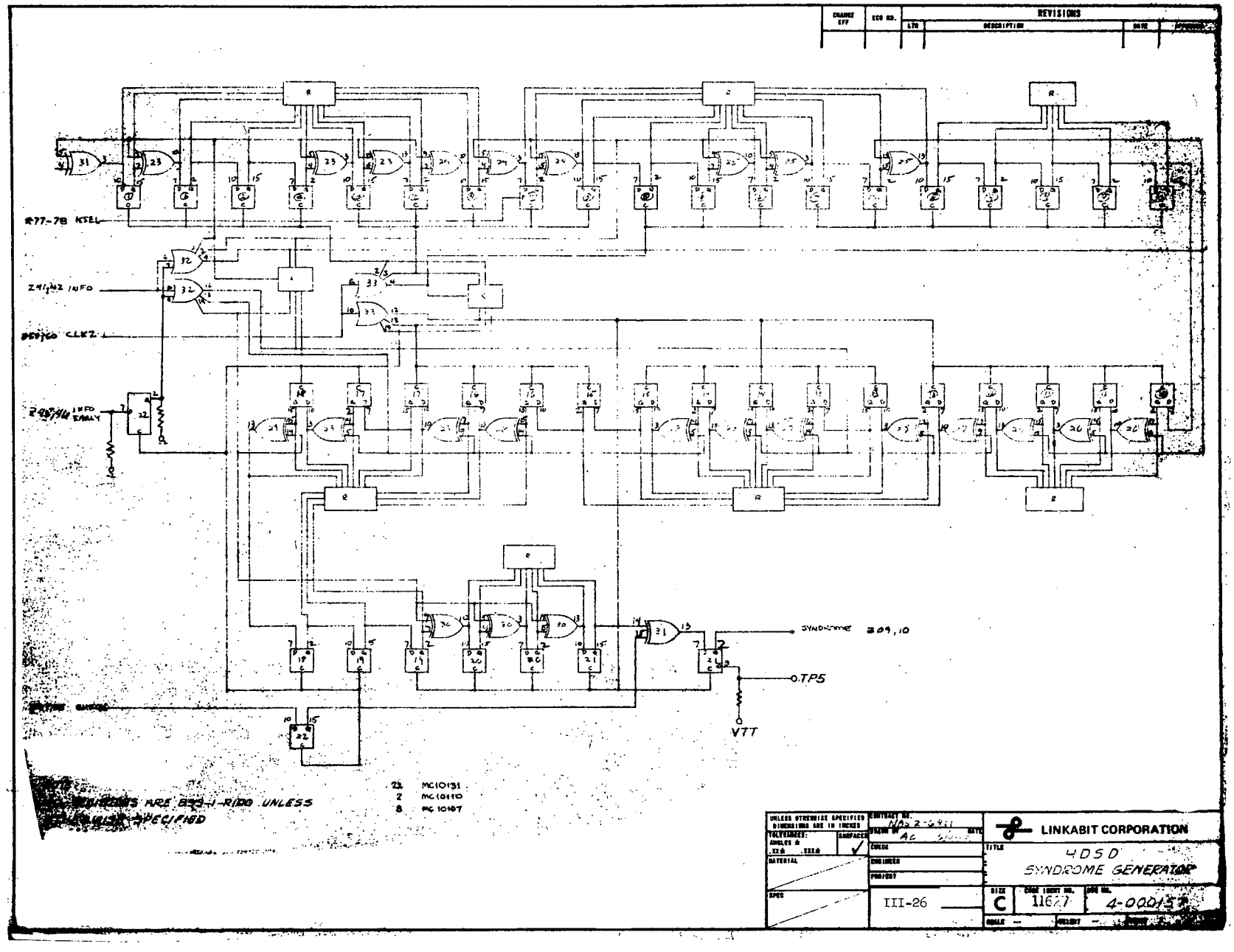
LINKABIT CORPORATION
HDSD
ALGORITHM LOGIC
III-22
C
11627
4-000156

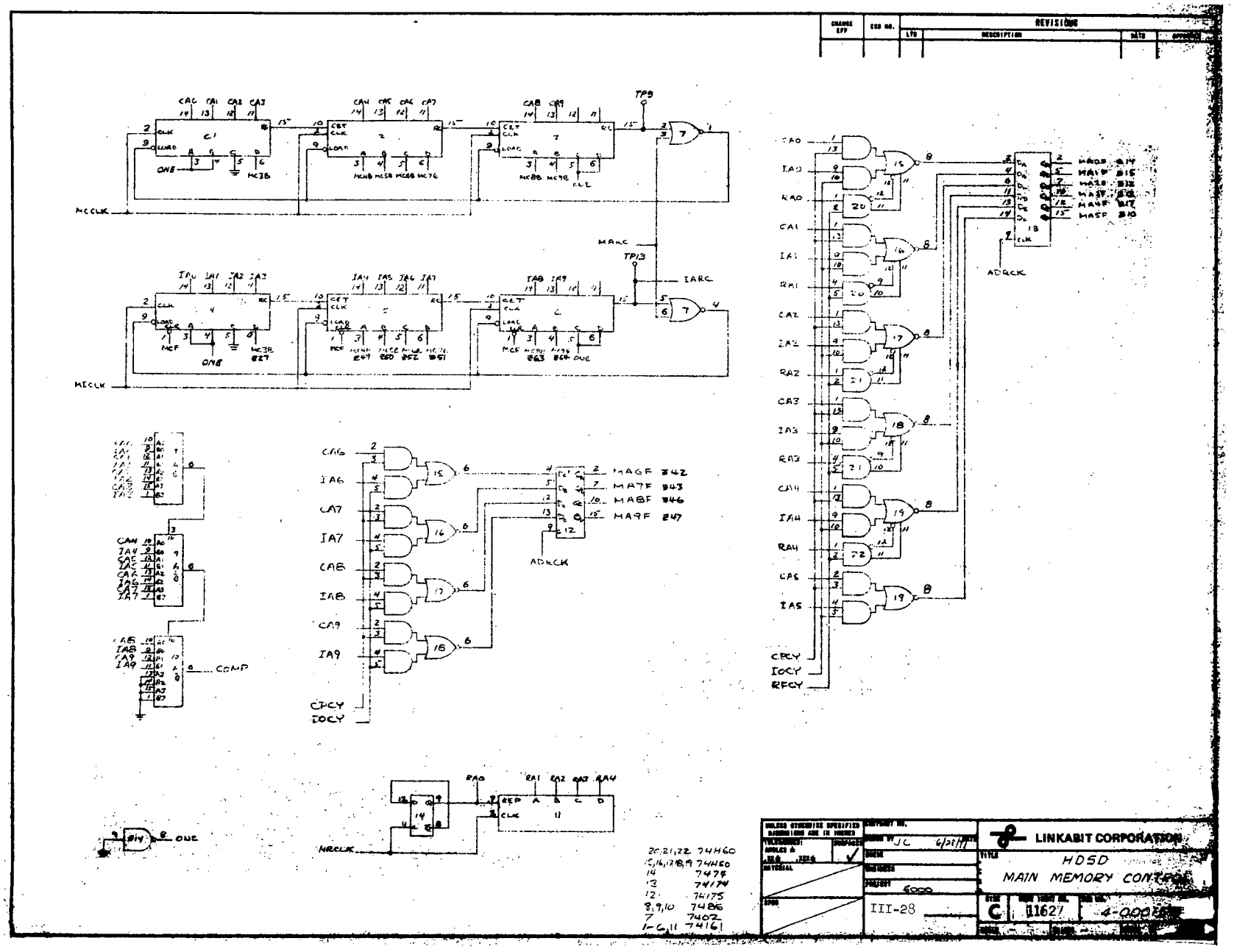

G41T
G16F
G40T
G18F
G17F
G41F
G42F
G43F
G44F
G45F
G46F
G47F
G48F
G49F
G50F
G51F
G52F
G53F
G54F
G55F
G56F
G57F
G58F
G59F
G60F
G61F
G62F
G63F
R69
R67
R71
R73
R72
R70
R128
R111
R147
R132
R127
R165
R142
R134
R141
R133
R135
R136
R164
R163
R166
R47
R48
R50
R75
R139
R24
R110
R46
R11
R29
R51
R49
R27
-2V
I.C. 60-72
MC 1660 60,61,63-72
MC 1662 62
2/7/72 kdb
LINKABIT CORPORATION
HDSD
ALGORITHM LOGIC
III-23
C



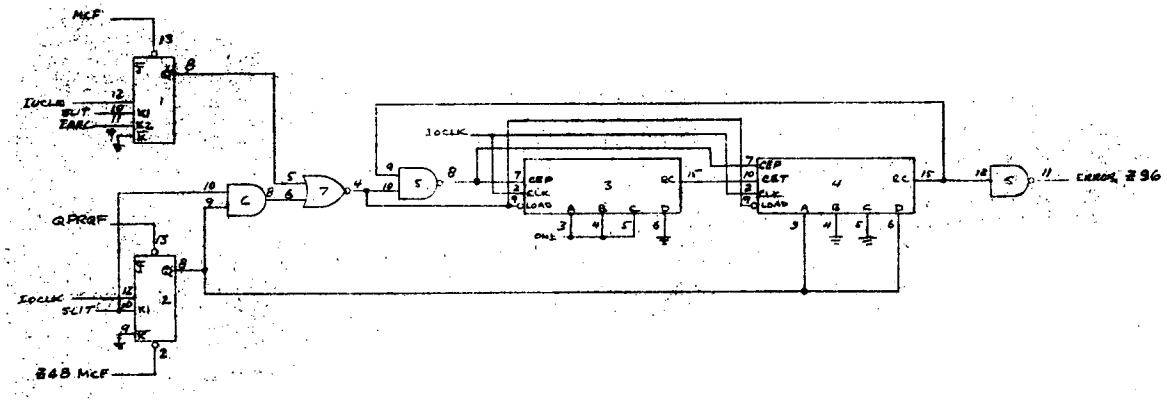

REVISIONS
R3 -8V
R2 -8V
R6
R5 -2V
R9
R13
R25
R7 -2V
R8 -2V
R4 -2V
K2T6
K2T6
K2T6
IC85
OVFL
MSF
MSF1
OVFL1
OVFL2
OVFL3
G23F
R143
R129
R199 -8V
R138
R130 -2V
R137 -2V
R162
R196
R195
R197 -2V
R198 -2V
R200
R18 -2V
M1DF
M9F
G23F
G21F
K2T1
K2T7
K2T1
MSF
M1DF
M9DF
M9F
G23F
G21F
M12
R18
R200
OVFL
J29
R109
R108
R234
R14
-2
-2
-2
OVFL1
OVFL2
OVFL3
OVFL4
OVFL5
OVFL6
B13
J30
R145
-2V
109
B13T
B13F
K2T1
MC 1662 96-98, 103-108
MC 1670 93-95, 99-102, 107-109
MC 10110 108
I.C. 93-108
I.C.108
MC 10110
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± .XX ± .XXX ±
SURFACES
MATERIAL
SPEC
CONTRACT NO.
DRAWN BY
DATE
CHECK
ENGINEER
PROJECT
III-25
LINKABIT CORPORATION
TITLE
HDSD
ALGORITHM LOGIC
SIZE C
CODE IDENT NO. 11627
DWG NO. 4-000156
SCALE —
SHEET 6 OF 6


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
R77-78 KSEL
Z4/Z42 INFO
CLK2
INFO EARLY
SYNDROME 309,10
OTP5
VTT
23 MC10131
2 MC10110
8 MC10107
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
.XX± .XXX±
SURFACES
MATERIAL
SPEC
CONTRACT NO.
DRAWN BY AC
DATE
CHECK
ENGINEER
PROJECT
III-26
LINKABIT CORPORATION
TITLE
4DSD
SYNDROME GENERATOR
SIZE C
CODE IDENT NO. 11627
DWG NO. 4-000157
SCALE —
WEIGHT —
SHEET

38	74H11
37	74LS04
35,36	7408
34	MC9601
32	74S11
31	74S20
29,30	74S74
28	74S10
27	74H74
24,25,26	74H76
23	74H05
22	74H21
20	74J2
18,23	7420
15,19	7410
13,14	7408
8,9,10,11,12,17	7400
7,16	7404
6	74H04
4,5	74141
1,2,3,21	7402


REVISIONS
CHANGE EFF
ECO NO.
LTR
DESCRIPTION
DATE
APPROVED
CA0 CA1 CA2 CA3
CA4 CA5 CA6 CA7
CA8 CA9
TP9
MCCLK
MARC
IA0 IA1 IA2 IA3
IA4 IA5 IA6 IA7
IA8 IA9
TP13
IARC
MICLK
CA6
IA6
CA7
IA7
CA8
IA8
CA9
IA9
CPCY
IDCY
MAGF #42
MA7F #43
MA8F #46
MA9F #47
ADRCK
CA0
IA0
RA0
CA1
IA1
RA1
CA2
IA2
RA2
CA3
IA3
RA3
CA4
IA4
RA4
CA5
IA5
RFCY
MA0F #14
MA1F #15
MA2F #32
MA3F #33
MA4F #47
MA5F #10
COMP
ONE
RA0 RA1 RA2 RA3 RA4
MRCLK
20,21,22 74H60
5,16,17,18,19 74H60
14 7478
13 74174
12 74175
8,9,10 7486
7 7402
1-6,11 74161
LINKABIT CORPORATION
TITLE
HDSD
MAIN MEMORY CONTROL
SIZE
C
11627
4-000
III-28
6000
4/21/77

CHANGE LTR	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



A	7402
B	7403
C	7486
D	7486
E	74161
F	7470

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± .XX ± .XXX ±
SURFACES ✓
MATERIAL
SPEC

CONTRACT NO.
DRAWN BY DATE
CHECK
ENGINEER
PROJECT 6000

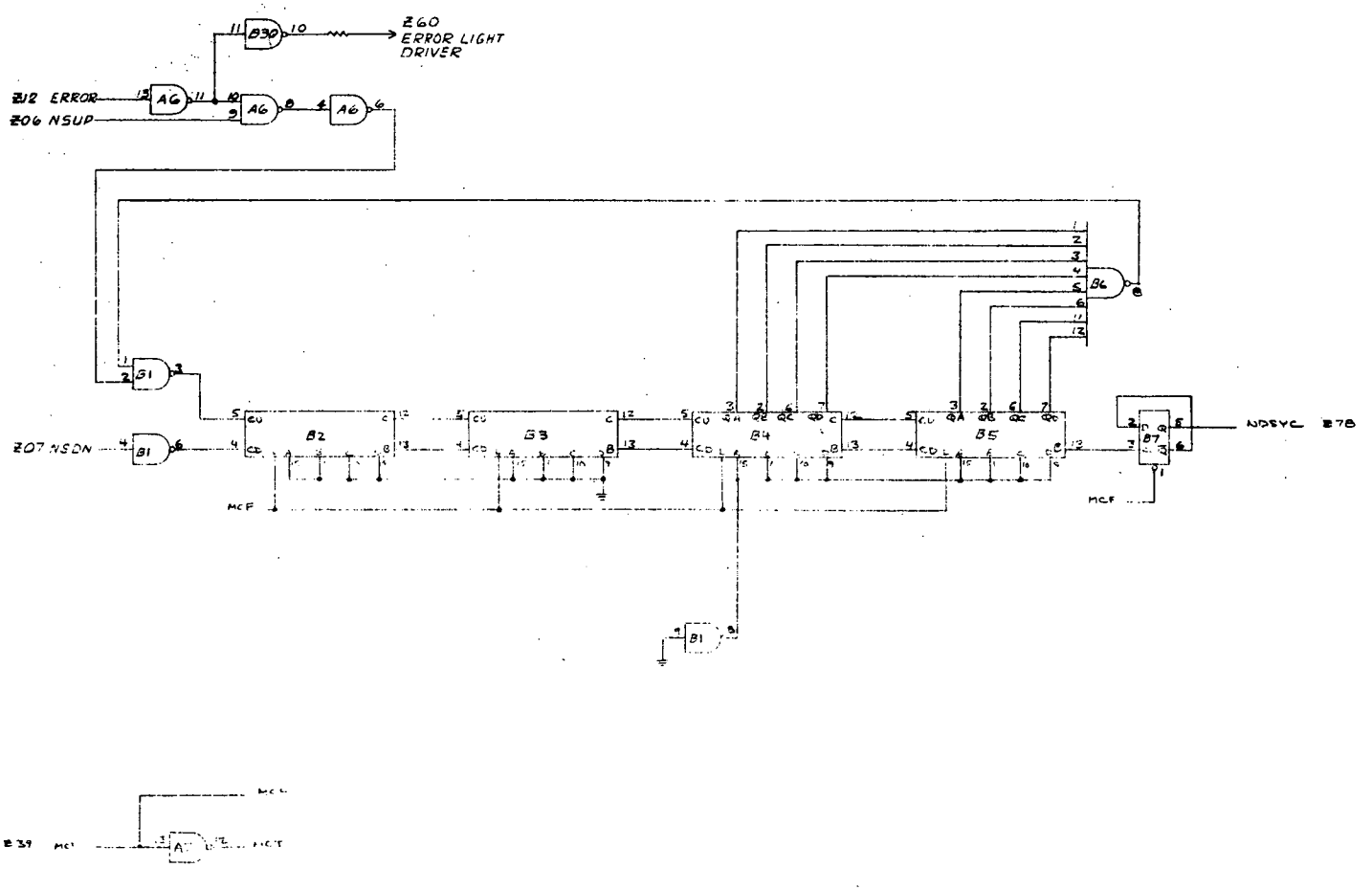
III-29

LINKABIT CORPORATION

TITLE HDSD MAIN MEMORY CONTROL

SIZE C | CODE IDENT NO. 11627 | DWG NO. 4-000158

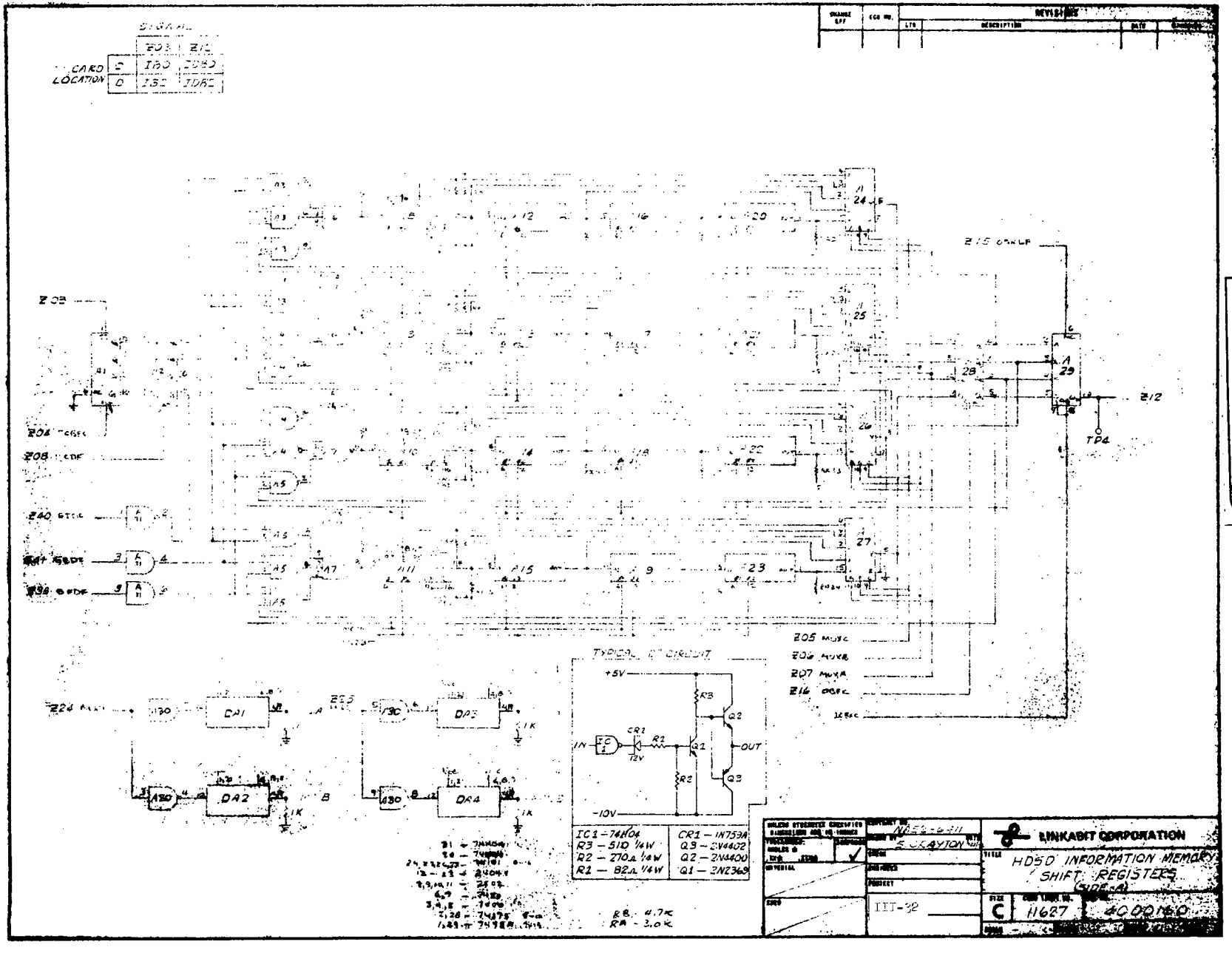
SCALE — WEIGHT — SHEET — REV

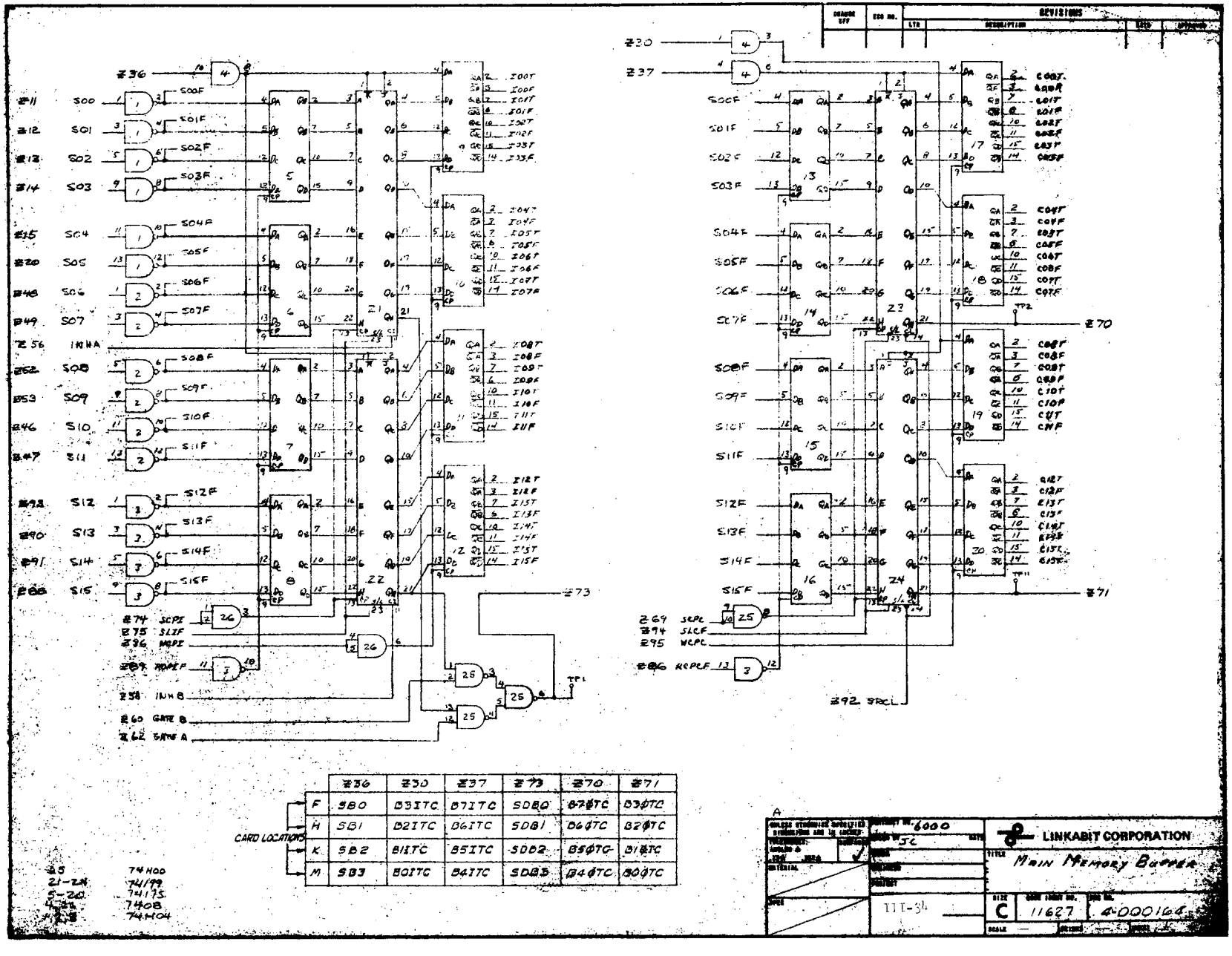


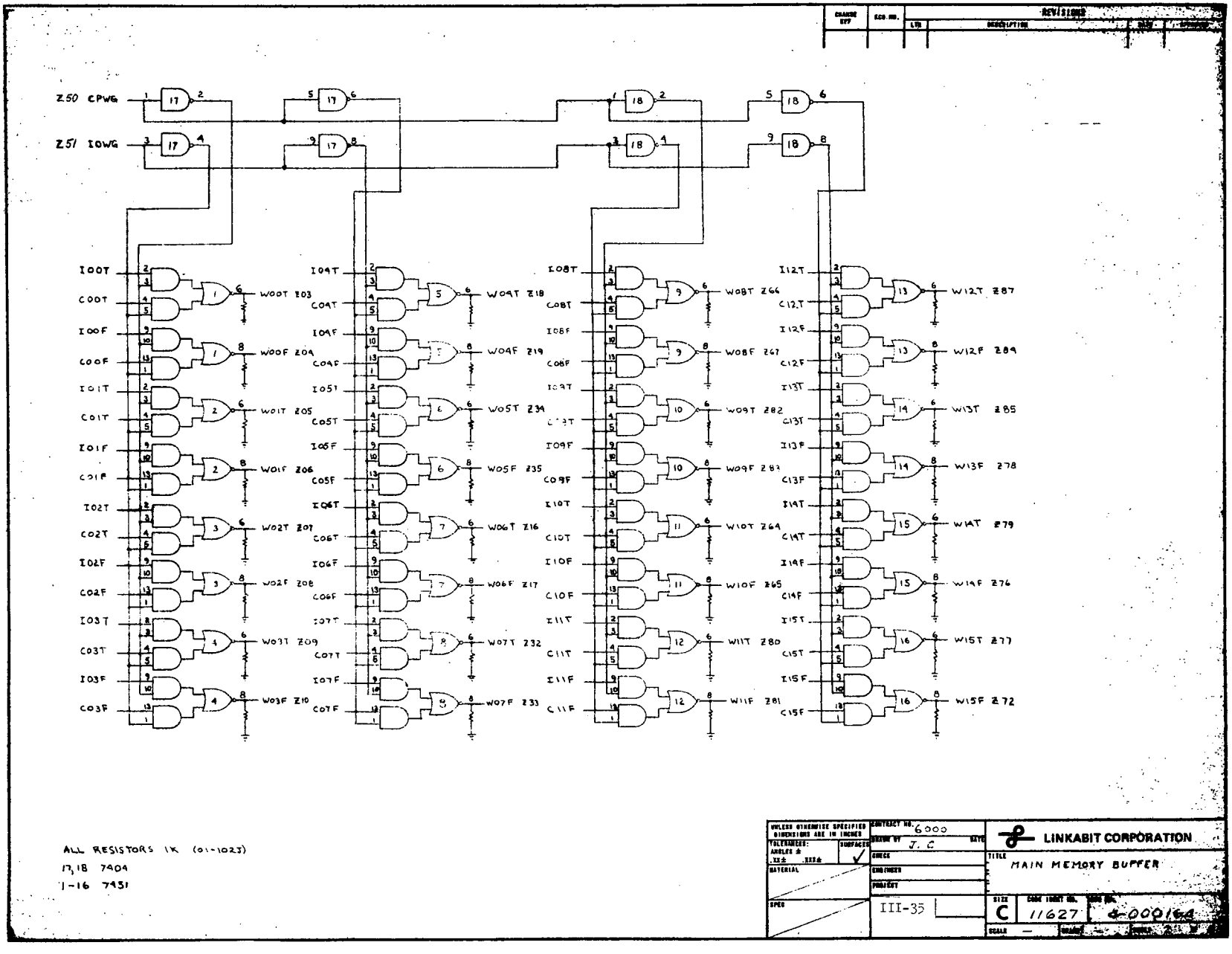
7 — 7474
6 — 7430
2,3,4,5 — 74193
1 — 7400

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. 6000	LINKABIT CORPORATION	SIZE C
TOLERANCES: ANGLES ± .XX ± .XXX	DRAWN BY JC DATE	TITLE HD5D INFO MEMORY CONTROL	CODE IDENT NO. 11627
SURFACES ✓	CHECK		DWG NO. 4000159
MATERIAL	ENGINEER		SCALE — WEIGHT — SHEET 2 OF 2
SPEC	PROJECT III-31		

CARD E




Z36
Z30
Z37
Z70
Z71
Z73
Z92 SRCL
S00
S01
S02
S03
S04
S05
S06
S07
S08
S09
S10
S11
S12
S13
S14
S15
INHA
INHB
GATE B
GATE A
SCPE
SLCE
WCPE
RCPE
SCPL
SLCF
WCPL
RCPLF
CARD LOCATIONS
Z36 Z30 Z37 Z73 Z70 Z71
F SB0 B3ITC B7ITC SDB0 B7ØTC B3ØTC
H SB1 B2ITC B6ITC SDB1 B6ØTC B2ØTC
K SB2 B1ITC B5ITC SDB2 B5ØTC B1ØTC
M SB3 B0ITC B4ITC SDB3 B4ØTC B0ØTC
74H00
74199
74175
7408
74H04
LINKABIT CORPORATION
Main Memory Buffer
111-34
C
11627
4-000166

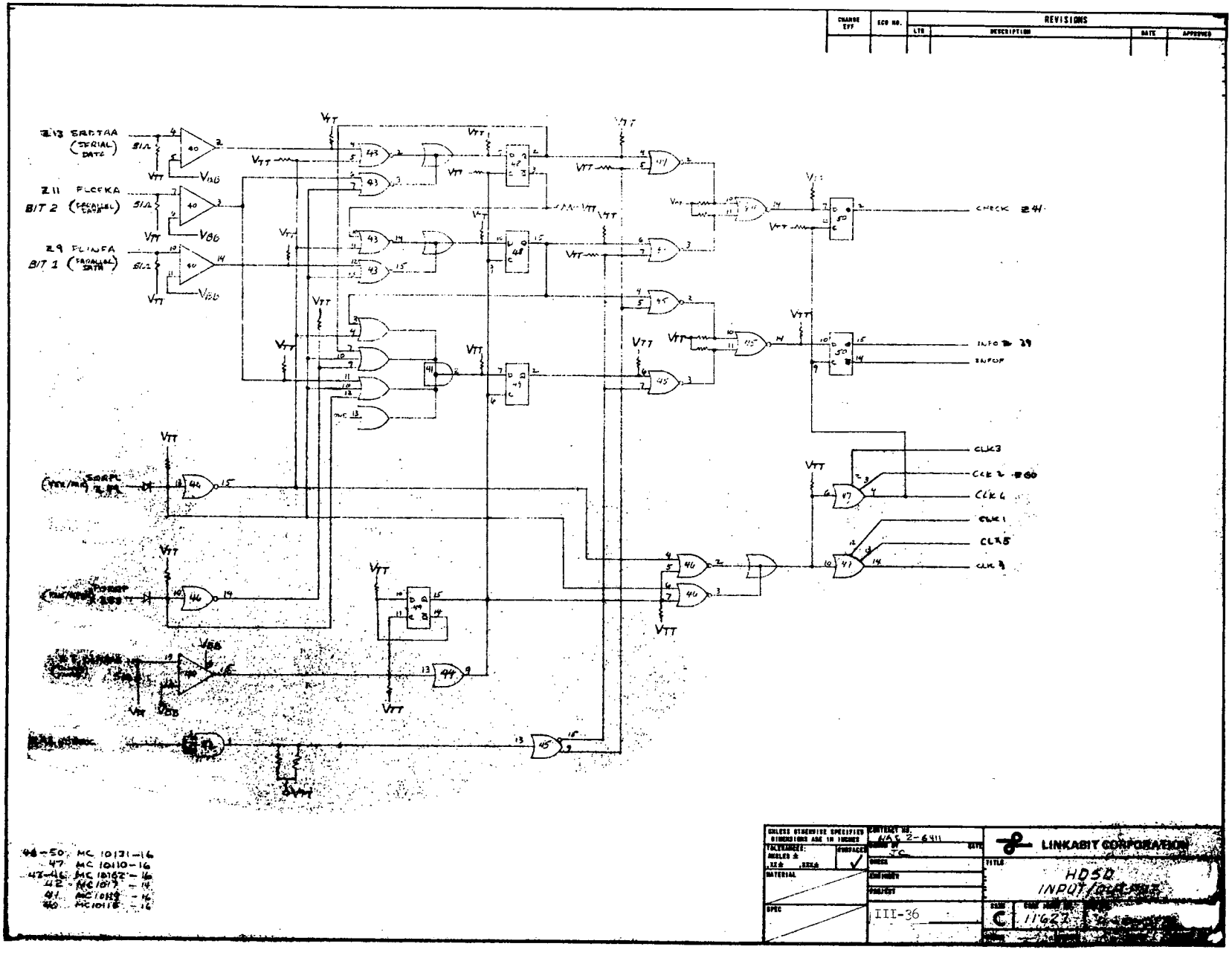


ALL RESISTORS 1K (01-1023)

17,18 7404

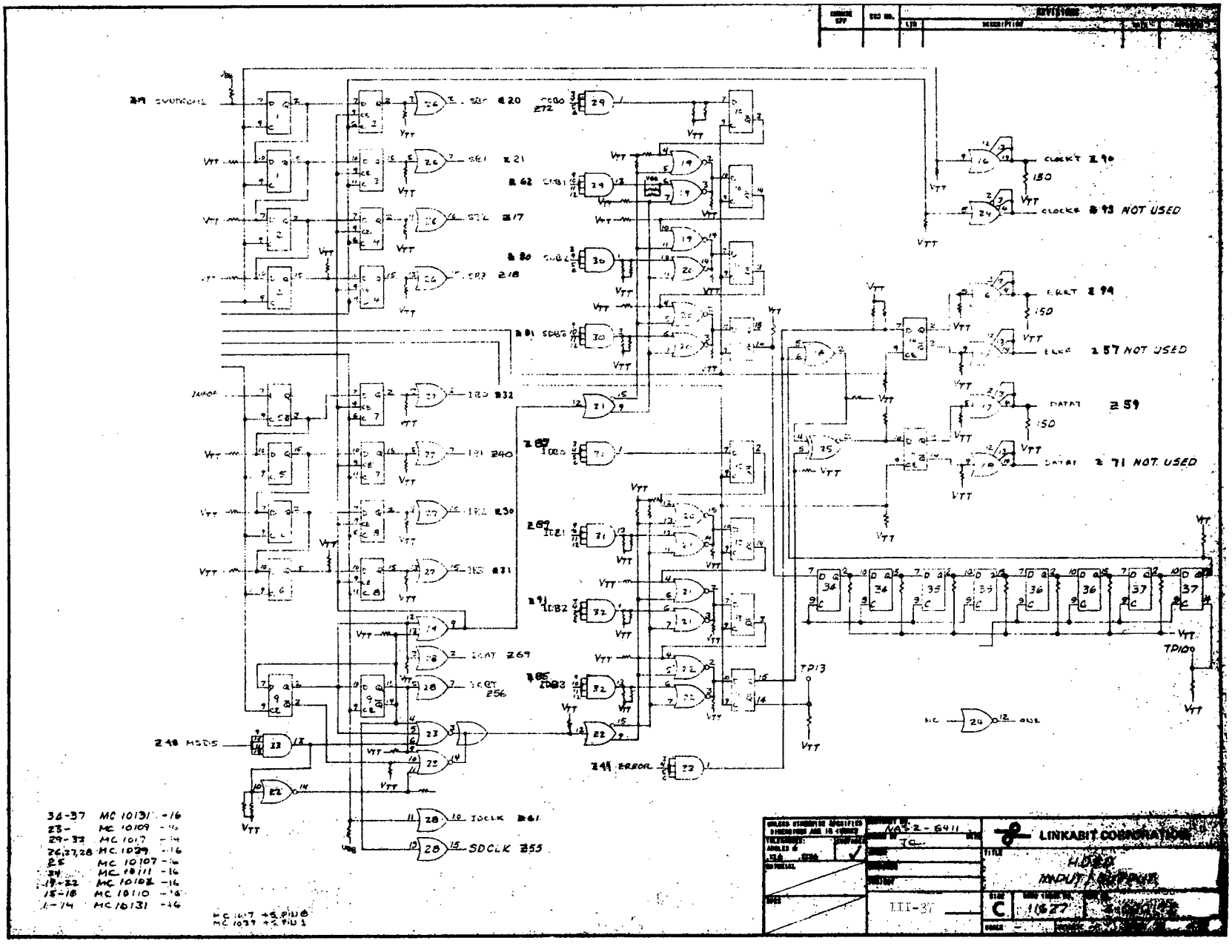
1-16 7451

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. 6000	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX ± .XXX ±	DRAWN BY J. C DATE	TITLE MAIN MEMORY BUFFER	
SURFACES ✓	CHECK		
MATERIAL	ENGINEER		
SPEC	PROJECT III-35	SIZE C	CODE IDENT NO. 11627
		SCALE —	SHEET —



40-50, MC 10131-16
47 MC 10110-16
42-46 MC 10162-16
42 MC 10173-16
41 MC 10113-16
40 MC 10116-16

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±, XX ±, XXX ±
SURFACES
MATERIAL
SPEC
CONTRACT NO. NAS 2-6411
DRAWN W
DATE
CHECKED
ENGINEER
PROJECT
III-36
LINKABIT CORPORATION
TITLE
HDSD
INPUT/OUTPUT
SIZE C
11623



APPENDIX IV - WIRE LIST

TABLE OF CONTENTS

BUG	LOC	PINS	ID
A01	H10	16	10131
A02	H 1	16	10131
A03	F10	16	10131
A04	F 1	16	10131
A05	H28	16	10131
A06	H19	16	10131
A07	F28	16	10131
A08	F19	16	10131
A09	D58	16	10131
A10	H37	16	10131
A11	H46	16	10131
A12	H55	16	10131
A13	H64	16	10131
A14	P37	16	10131
A16	M55	16	10110
A17	M37	16	10110
A18	M46	16	10110
A19	F37	16	10102
A20	F46	16	10102
A21	F55	16	10102
A22	F64	16	10102
A23	D49	16	10109
A24	M64	16	10111
A25	P46	16	10107
A26	B 5	16	1039
A27	B23	16	1039
A28	D40	16	1039
A29	B40	14	1017
A30	B48	14	1017
A31	B56	14	1017
A32	B64	14	1017
A33	B32	14	1017
A40	D14	16	10115
A41	K10	16	10119
A42	D32	14	1017
A43	K19	16	10102
A44	P19	16	10102

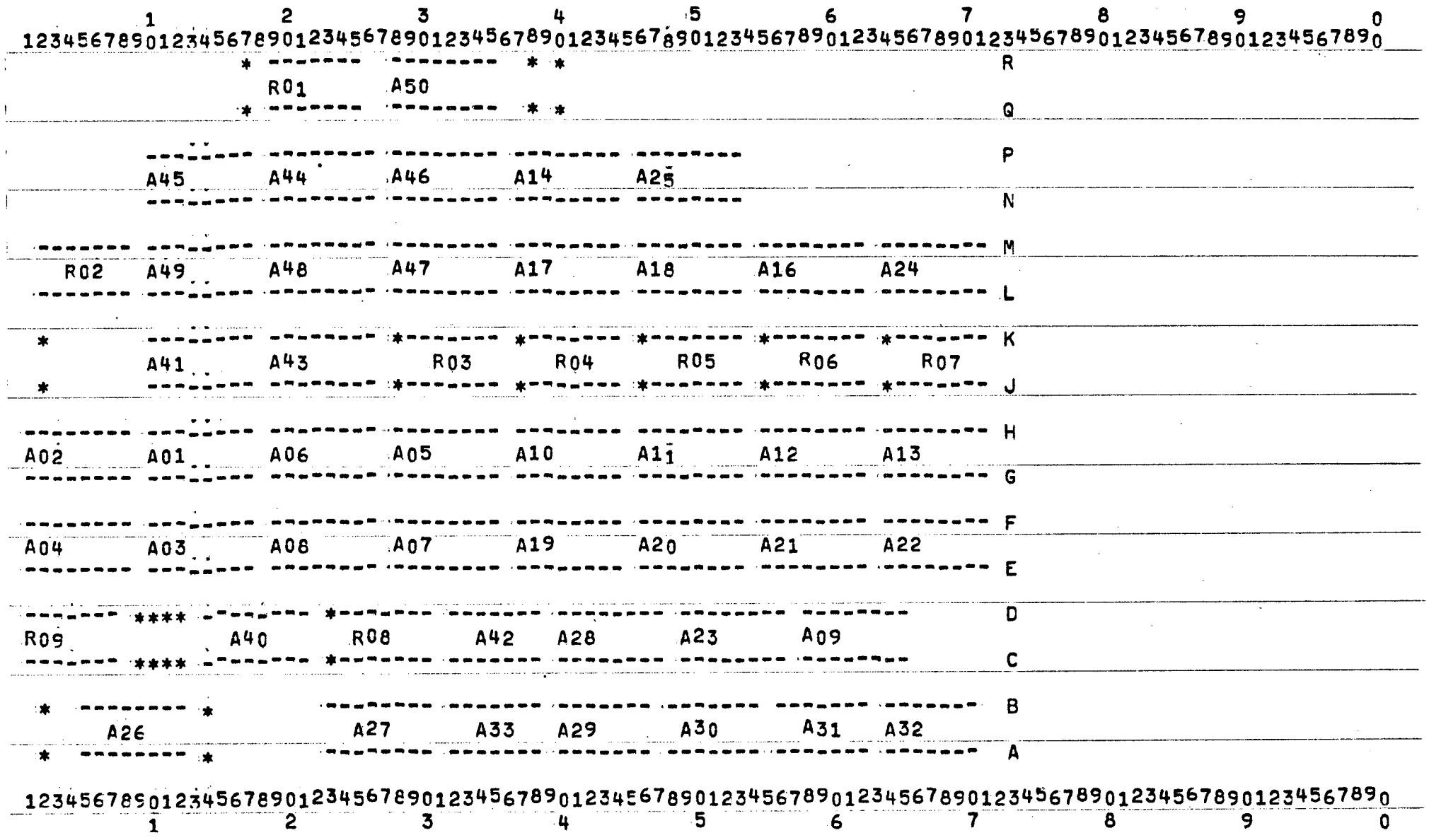
```
A45 P10 16 10102    Input Output
A46 P28 16 10102
A47 M28 16 10111
A48 M19 16 10131
A49 M10 16 10131
A50 R28 16 10131
R01 R19 14 899-1-150
R02 M 2 14 899-1-150
R03 K29 14 899-1-150
R04 K38 14 899-1-150
R05 K47 14 899-1-150
R06 K56 14 899-1-150
R07 K65 14 899-1-150
R08 D24 14 899-1-150
R09 D 1 14 899-1-150
R10 D 9  2 110
R11 D10  2 110
R12 D11  2 110
R13 D12  2 110
CR1 R38  2 914
CR2 R40  2 914
C01 B 2  2 .01
C02 K 2  2 .01
C03 R17  2 .01
C04 K28  2 .01
C05 K37  2 .01
C06 K46  2 .01
C07 K55  2 .01
C08 K64  2 .01
C09 D23  2 .01
C10 B14  2 .01
END   0  0
```

PARTS COUNT Input Output

10131	17
10110	3
10102	8
10109	1
10111	2
10107	1
1039	3
1017	6
10115	1
10119	1
899-1-150	9
110	4
914	2
.01	10

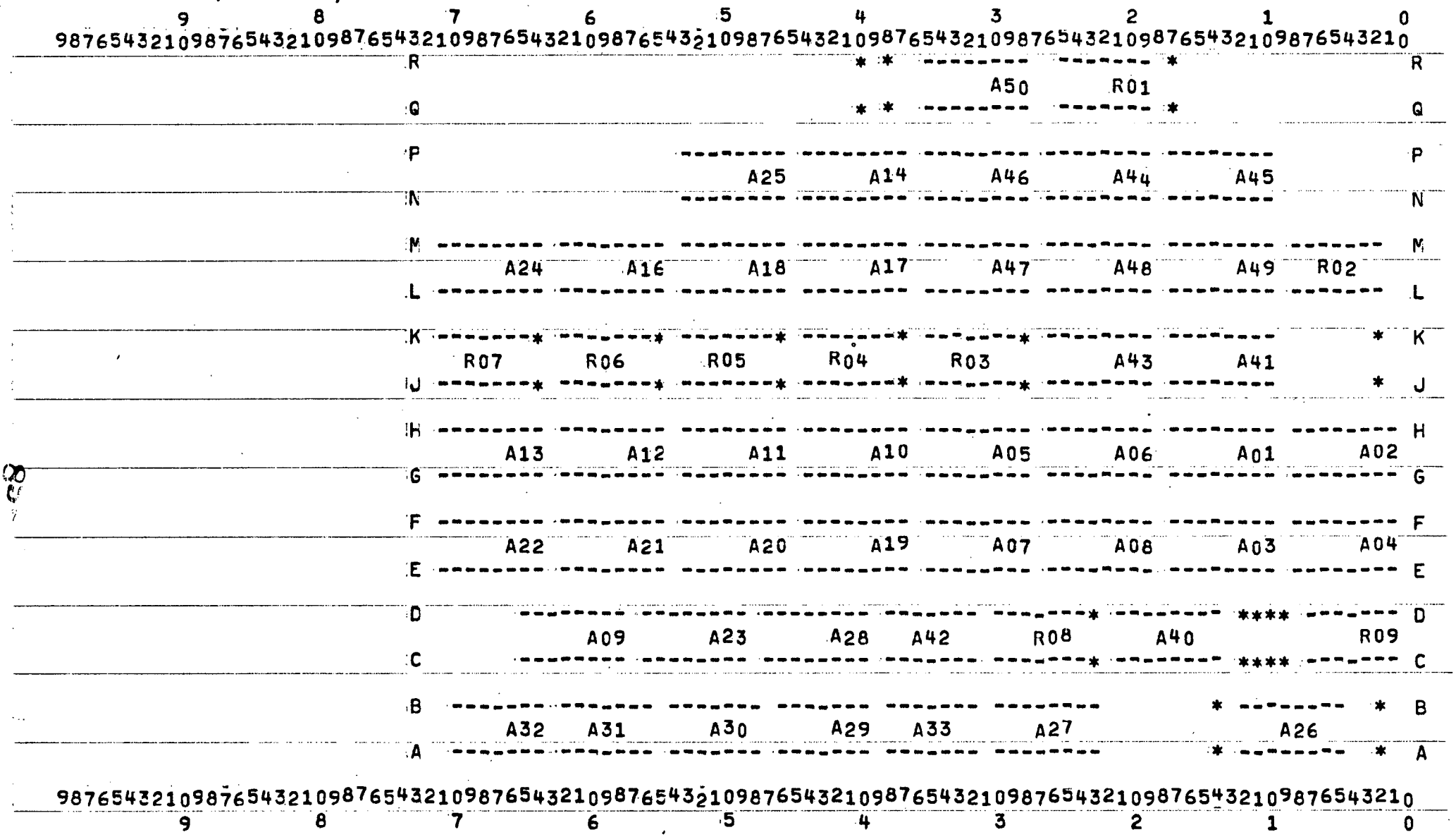
Input Output

PIN MAP -- PIN 1 IS AT UPPER LEFT



Input Output

BUG MAP -- PIN 1 IS AT UPPER RT



THERE ARE 68 BUGS, CONSISTING OF
0 8-PIN BUGS
15 14-PIN BUGS

37 16-PIN BUGS
0 24-PIN BUGS

SYNDROME GENERATOR JOB 6000

W L - 9 9 REV ECO 22 AUG 72 PINS-DOWN

BUG	LOC	PINS	ID
A01	B19	16	10131
A02	B28	16	10131
A03	B37	16	10131
A04	B46	16	10131
A05	B55	16	10131
A06	D64	16	10131
A07	F64	16	10131
A08	H64	16	10131
A09	K64	16	10131
A10	M64	16	10131
A11	P64	16	10131
A12	P55	16	10131
A13	P46	16	10131
A14	P37	16	10131
A15	P28	16	10131
A16	P19	16	10131
A17	M10	16	10131
A18	K10	16	10131
A19	H10	16	10131
A20	F10	16	10131
A21	D10	16	10131
A22	B10	16	10131
A23	D28	16	10107
A24	D46	16	10107
A25	F55	16	10107
A26	M55	16	10107
A27	M46	16	10107
A28	M28	16	10107
A29	M19	16	10107
A30	F19	16	10107
A31	D19	16	10107
A32	F28	16	10110
A33	F37	16	10110
A34	H28	16	10110
R01	D 2	14	899-1-150
R02	D38	14	899-1-150
R03	D56	14	899-1-150

Syndrome Generator

```
R04 K56 14 899-1-150
R05 R65 14 899-1-150
R06 M38 14 899-1-150
R07 P11 14 899-1-150
R08 H20 14 899-1-150
C01 D 1  2 0.01
C02 D37  2 0.01
C03 D55  2 0.01
C04 K55  2 0.01
C05 R64  2 0.01
C06 M37  2 0.01
C07 P10  2 0.01
C08 H19  2 0.01
C09 H41  2 0.01
C10 B 6  2 0.01
C09 H37  2 RC07-51
C10 H39  2 RC07-51
C11 B 8  2 RC07-51
END   0  0
```

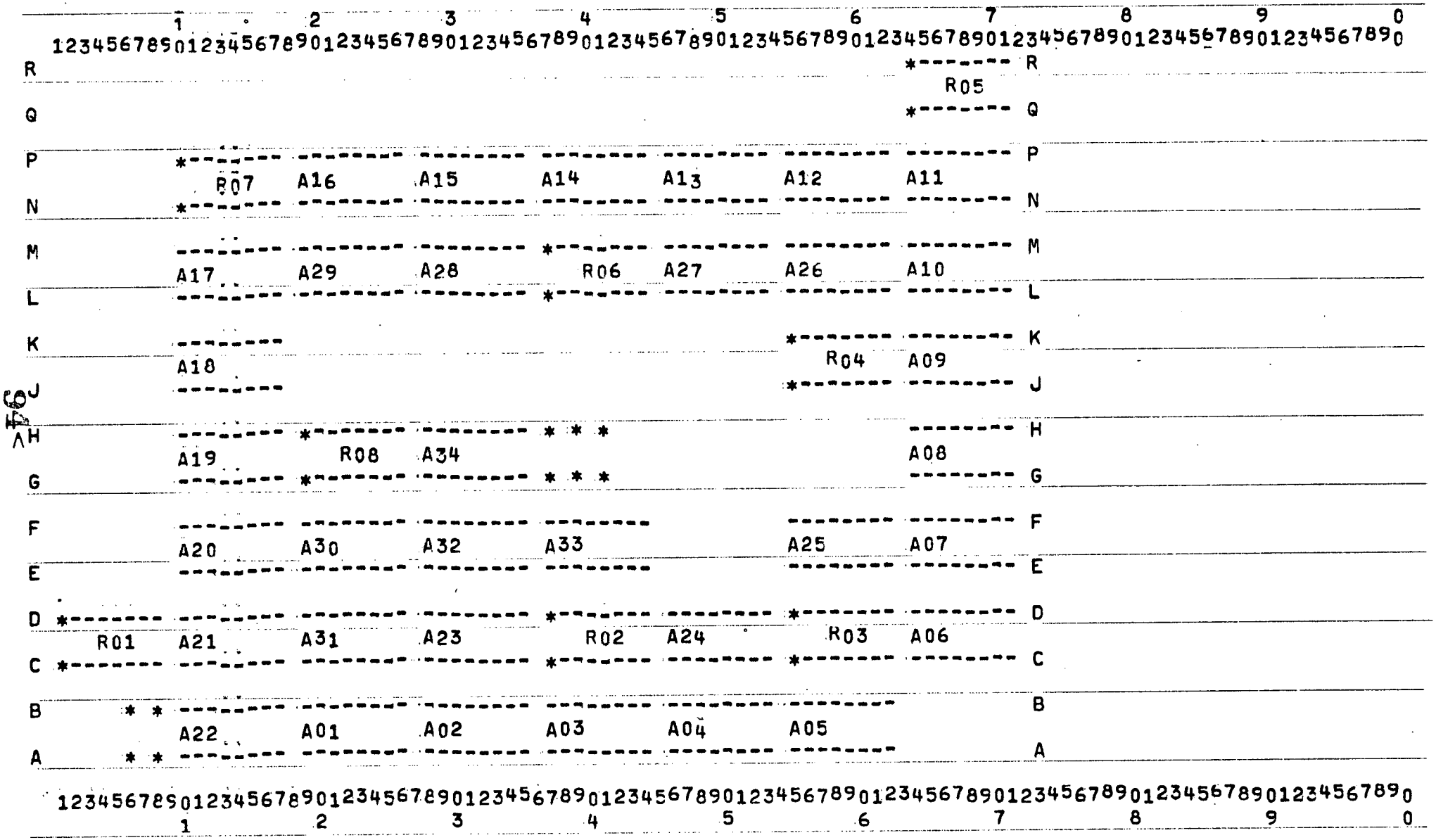
26

PARTS FOUNT Syndrome Generator

10131	22
10107	9
10110	3
899-1-150	8
0.01	10
RC07-51	3

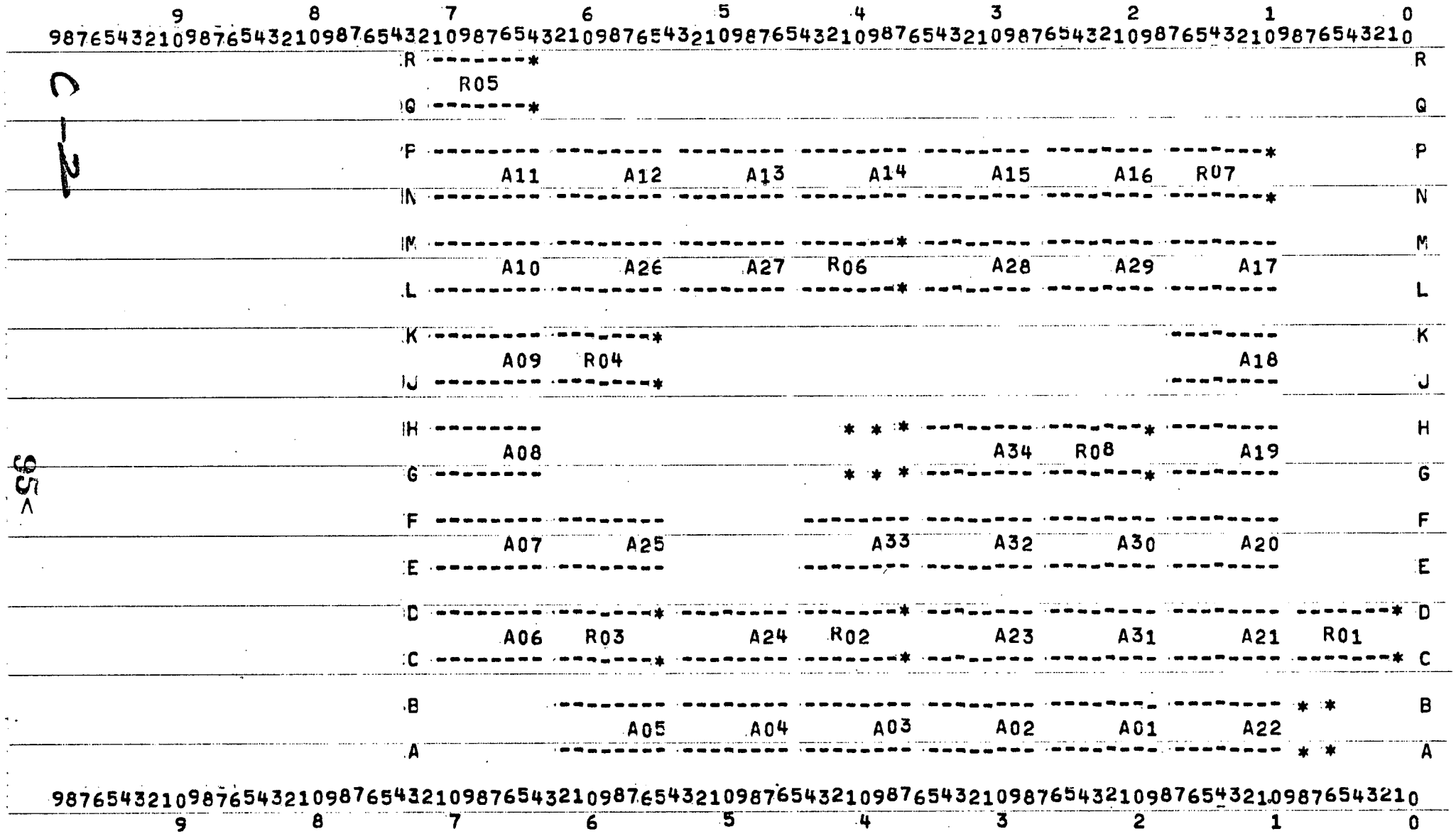
SYNDROME GENERATOR

PIN MAP -- PIN 1 IS AT UPPER LEFT



Syndrome Generator

BUG MAP -- PIN 1 IS AT UPPER RT



THERE ARE 55 BUGS, CONSISTING OF
0 8-PIN BUGS
8 14-PIN BUGS

34 16-PIN BUGS
n 24-PIN BUGS

SYNDROME GENERATOR

INFO MEMORY SHIFT REG, A SIDE JOB 6000

W L - 1 0 REV ECO 22 AUG 72 PINS-DOWN

BUG	LOC	PINS	ID
A01	B 3	14	7495A
A02	B11	16	74175
A03	D28	14	7400
A04	D20	14	07400
A05	D12	14	07400
A06	F24	14	07420
A07	F 6	14	07420
A08	H28	16	2502R
A09	H19	16	2502R
A10	H10	16	2502R
A11	H 1	16	2502R
A12	K28	8	2504V
A13	K19	8	2504V
A14	K10	8	2504V
A15	K 1	8	2504V
A16	M28	8	2504V
A17	M19	8	2504V
A18	M10	8	2504V
A19	M 1	8	2504V
A20	P28	8	2504V
A21	P19	8	2504V
A22	P10	8	2504V
A23	P 1	8	2504V
A24	R28	16	74151
A25	R19	16	74151
A26	R10	16	74151
A27	R 1	16	74151
A28	T15	16	74175
A29	V15	14	7495A
A30	B20	14	74H04
A31	B28	14	74H04
DA1	T25	22	CLKDR
A31	B28	14	74H04
DA2	V25	22	CLKDR
DA3	T 2	22	CLKDR
DA4	V 2	22	CLKDR
R01	F32	2	04700

INFO memory shift Reg. A Sicle

R02	F22	2	04700
R03	F14	2	04700
R04	F 4	2	04700
R05	K34	2	04700
R06	K33	2	04700
R07	K35	2	04700
R08	K25	2	04700
R09	K24	2	04700
R10	K26	2	04700
R11	K16	2	04700
R12	K15	2	04700
R13	K17	2	04700
R14	K 7	2	04700
R15	K 6	2	04700
R16	K 8	2	04700
R17	M33	2	04700
R18	M24	2	04700
R19	M15	2	04700
R20	M 6	2	04700
R21	P34	2	04700
R22	P25	2	04700
R23	P16	2	04700
R24	P 7	2	04700
R31	F33	2	03000
R32	F21	2	03000
R33	F15	2	03000
R34	F 3	2	03000
R35	P33	2	03000
R36	P24	2	03000
R37	P15	2	03000
R38	P 6	2	03000
R39	F35	2	1K
R40	F 1	2	1K
R41	F36	2	1K
R42	F18	2	1K
C01	T36	2	CAP
C02	V36	2	CAP
C03	T13	2	CAP
C04	V13	2	CAP
C20	P 8	2	.01
C21	P17	2	.01
C22	P26	2	.01

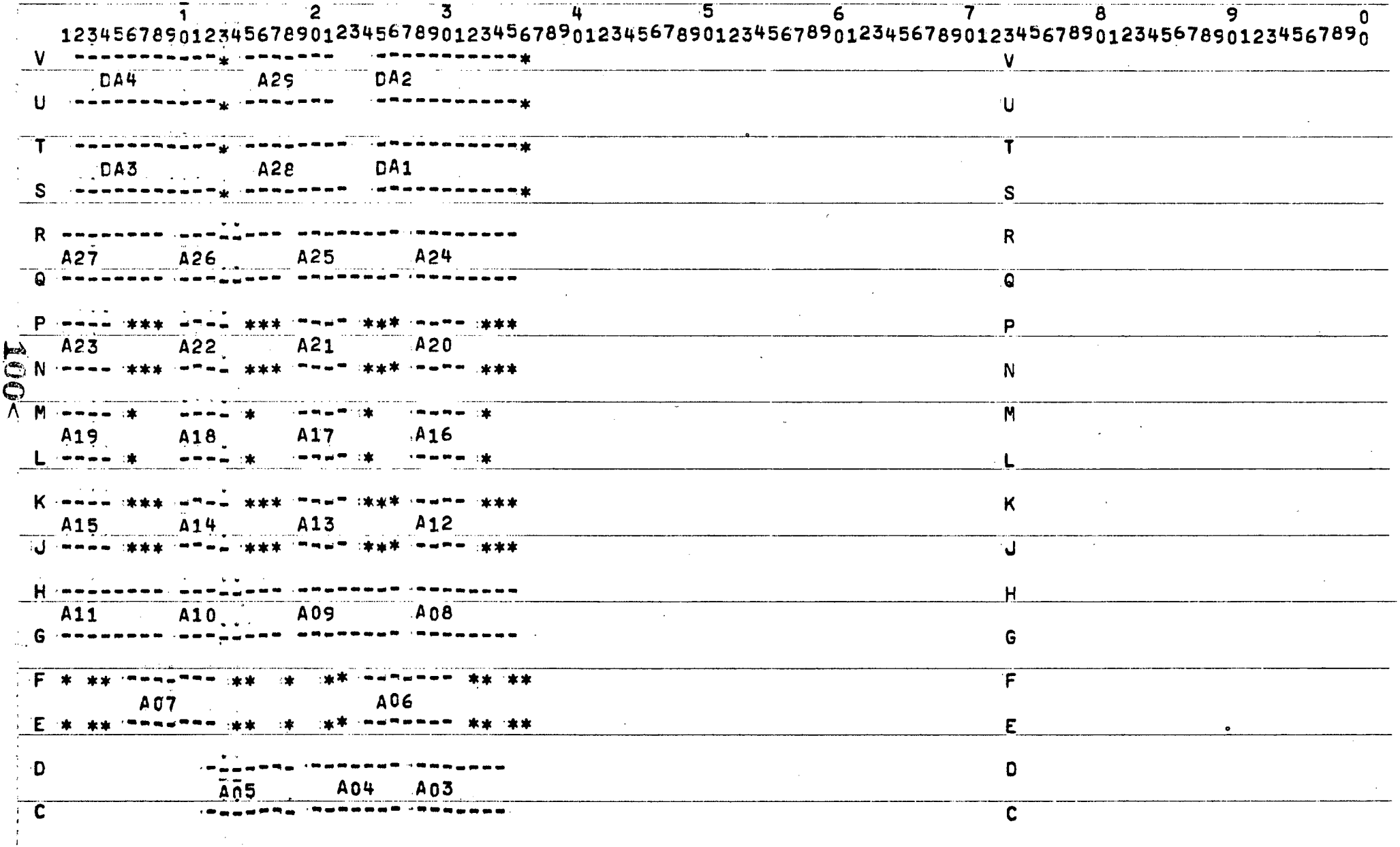
PARTS COUNT INFO memory shift Reg. A Side

7495A	2
74175	2
7400	1
07400	2
07420	2
2502B	4
2504V	12
74151	4
74H04	3
CLKDR	4
04700	24
03000	8
1K	4
CAP	4
.01	4

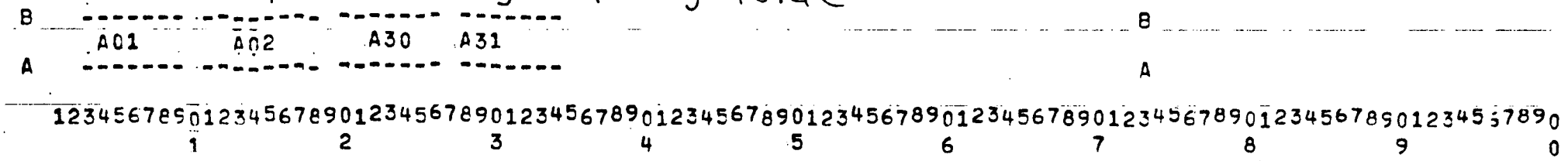
69 A

INFO memory SHIFT REG. A Side

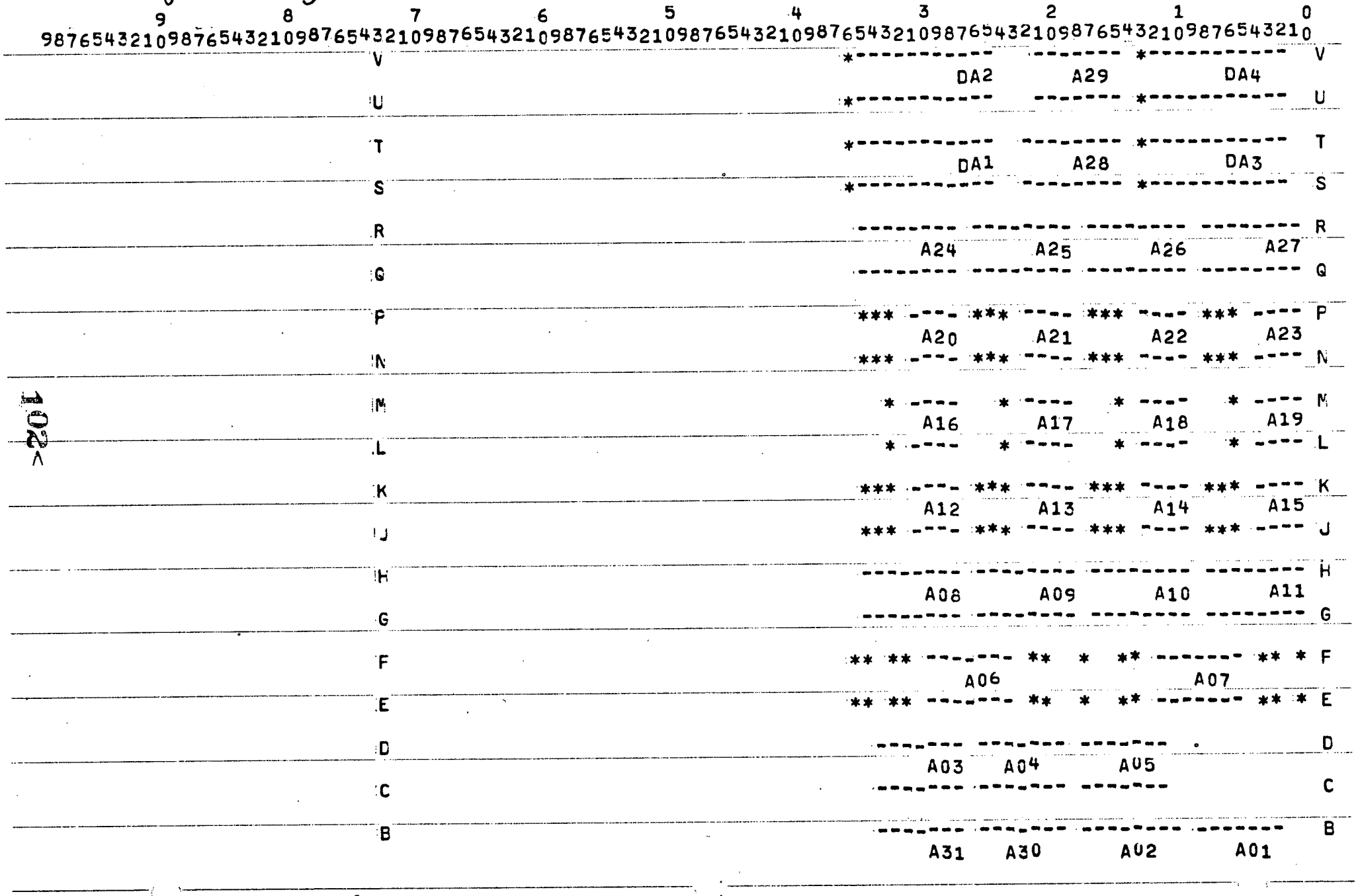
PIN MAP -- PIN 1 IS AT UPPER LEFT



INFO memory shift Reg Aside



INFO memory shift Reg. A side BUG MAP -- PIN 1 IS AT UPPER RT



102 V

```
A  Info Memory shift Reg. A side ------- ------- -------- -------  A
9876543210987654321098765432109876543210987654321098765432109876543210
         9        8        7        6        5        4        3        2        1        0

THERE ARE  80 BUGS, CONSISTING OF
           12  8-PIN BUGS
           10 14-PIN BUGS
           10 16-PIN BUGS
            0 24-PIN BUGS
```

INFO MEMORY SHIFT REG. B SIDE JOB 6000

W L - 1 0 REV ECO 22 AUG 72 PINS-DOWN

BUG	LOC	PINS	ID
A31	B28	14	74H04
B01	B39	14	7495A
B02	B47	16	74175
B03	D65	14	7400
B04	D57	14	07400
B05	D49	14	07400
B06	F60	14	07420
B07	F42	14	07420
B08	H64	16	2502B
B09	H55	16	2502B
B10	H46	16	2502B
B11	H37	16	2502B
B12	K64	8	2504V
B13	K55	8	2504V
B14	K46	8	2504V
B15	K37	8	2504V
B16	M64	8	2504V
B17	M55	8	2504V
B18	M46	8	2504V
B19	M37	8	2504V
B20	P64	8	2504V
B21	P55	8	2504V
B22	P46	8	2504V
B23	P37	8	2504V
B24	R64	16	74151
B25	R55	16	74151
B26	R46	16	74151
B27	R37	16	74151
B28	T50	16	74175
B29	V50	14	7495A
B30	B56	14	74H04
DB1	T60	22	CLKDR
DB2	V60	22	CLKDR
DB3	T37	22	CLKDR
DB4	V37	22	CLKDR
R47	F71	2	1K
R48	F37	2	1K

104 A

INFO MEMORY SHIFT REG. B. SIDE

R49	F70	2	1K
R50	F53	2	1K
R51	F68	2	04700
R52	F58	2	04700
R53	F50	2	04700
A54	F40	2	04700
R55	K70	2	04700
R56	K69	2	04700
R57	K71	2	04700
R58	K61	2	04700
R59	K60	2	04700
R60	K62	2	04700
R61	K52	2	04700
R62	K51	2	04700
R63	K53	2	04700
R64	K43	2	04700
R65	K42	2	04700
R66	K44	2	04700
R67	M69	2	04700
R68	M60	2	04700
R69	M51	2	04700
R70	M42	2	04700
R71	P70	2	04700
R72	P61	2	04700
R73	P52	2	04700
R74	P43	2	04700
R81	F69	2	03000
R82	F57	2	03000
R83	F51	2	03000
R84	F39	2	03000
R85	P69	2	03000
R86	P60	2	03000
R87	P51	2	03000
R88	P42	2	03000
C05	T71	2	CAP
C06	V71	2	CAP
C07	T48	2	CAP
C08	V48	2	CAP
C24	P44	2	.01
C25	P53	2	.01
C26	P62	2	.01
C27	P71	2	.01

405 ↓

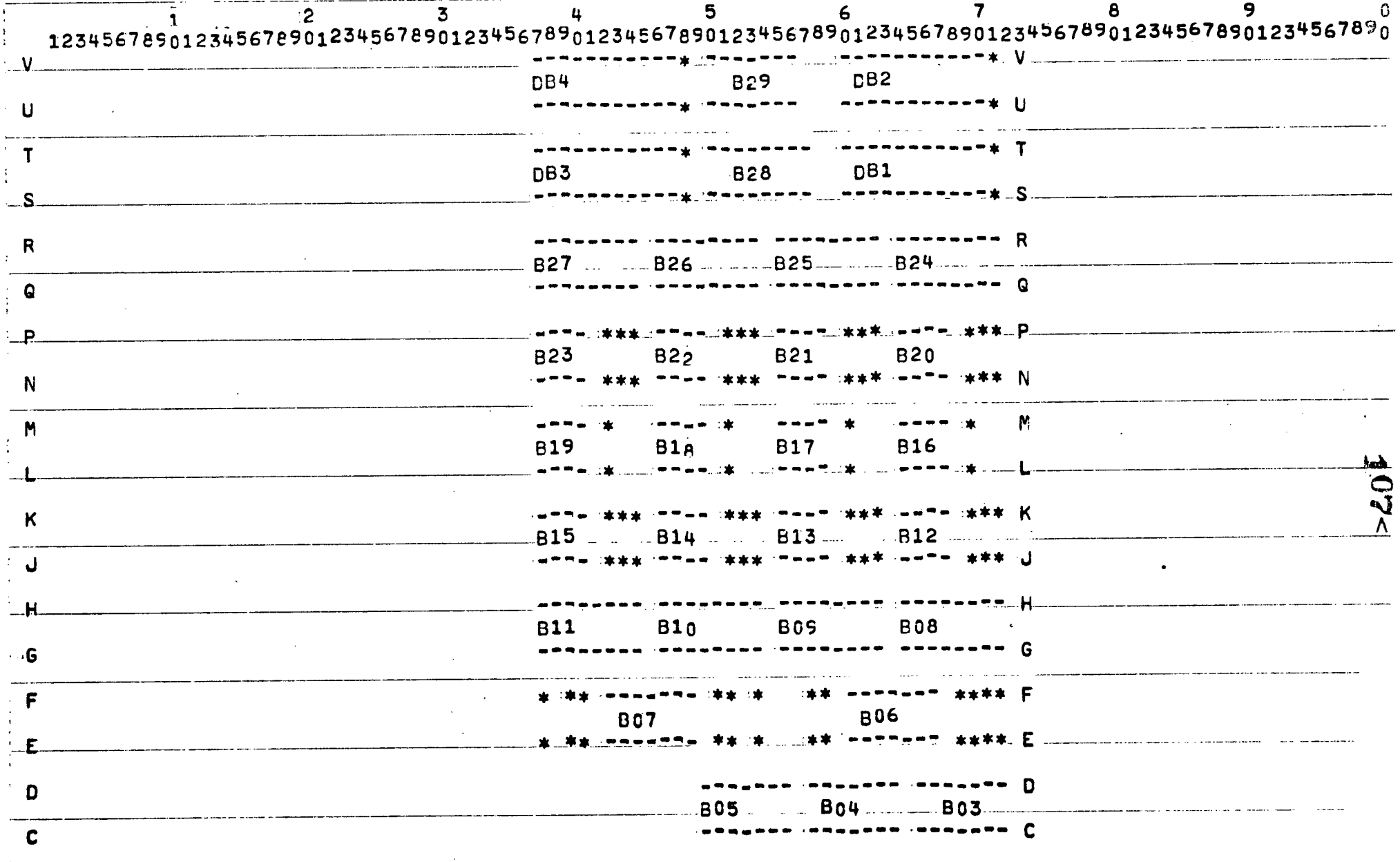
PARTS COUNT INFO MEMORY SHIFT REG B.SIDE

74H04	2
7495A	2
74175	2
7400	1
07400	2
07420	2
2502B	4
2504V	12
74151	4
CLKDR	4
1K	4
04700	24
03000	8
CAP	4
.01	4

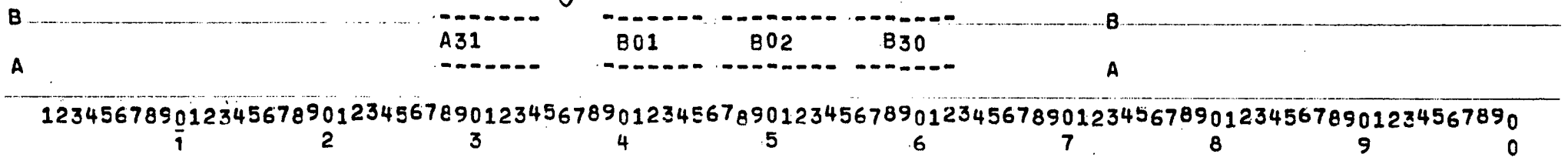
106-A

INFO memory shift REG. B. SIDE

PIN MAP -- PIN 1 IS AT UPPER LEFT

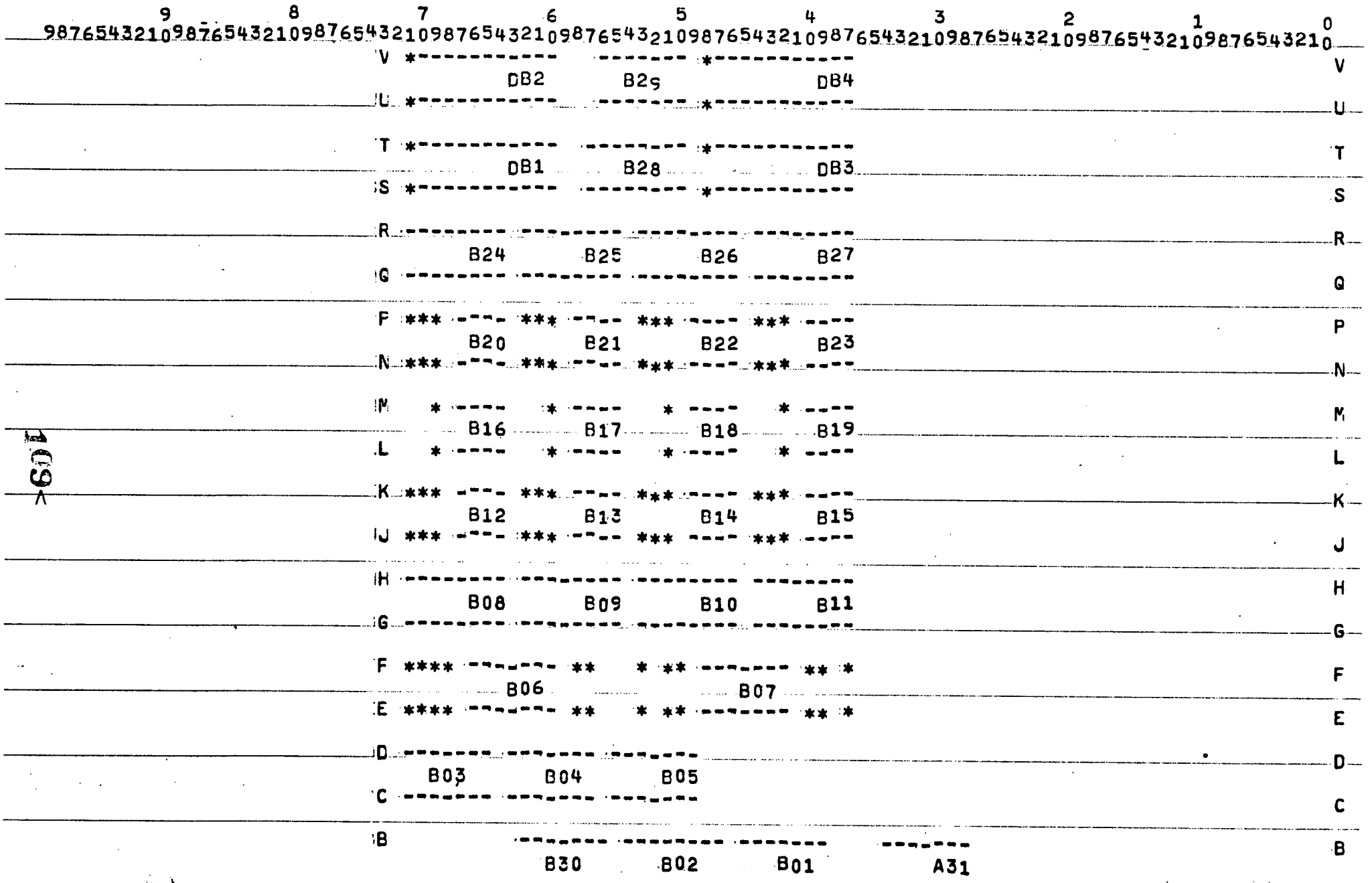


INFO memory shift Reg B. side



INFO memory shift REG B. Side

BUG MAP -- PIN 1 IS AT UPPER RT



A09

INFO memoryshift Reg. B Side

A ------- ------- ------- ------- A

98765432109876543210987654321098765432109876543210987654321098765432109876543210987654321098765432109876543210

9 8 7 6 5 4 3 2 1 0

THERE ARE 79 BUGS, CONSISTING OF
12 8-PIN BUGS
9 14-PIN BUGS
10 16-PIN BUGS
0 24-PIN BUGS

BUG	LOC	PINS	ID
R01	H62	2	330
R02	H60	2	5K
C01	K63	2	100PF
C02	H58	2	47PF
C03	M 7	2	500PF
A01	H41	16	7475
A02	F41	16	7475
A03	D52	16	7475
A04	K39	14	7400
A05	F25	14	7400
A06	B23	14	7400
A07	H33	14	7404
A08	M42	14	7408
A09	F50	14	7408
A10	K31	14	7410
A11	F33	14	7410
A12	K23	14	7420
A13	D36	14	7432
A14	B48	14	7432
A15	F58	14	7432
A16	M34	14	7430
A17	H16	14	74H21
A18	K55	14	7413
A19	M26	14	74H74
A20	K47	14	74H74
A21	D44	14	74H74
A22	D19	14	74H74
A23	H24	16	74H76
A24	B14	16	74163
A25	D27	16	74163
A26	F16	16	74163
A27	D10	16	74163
A28	B31	16	74163
A29	H50	14	9601
A30	B40	14	74H04
B01	M 9	14	7400
B02	K14	16	74193

```
B03 M17 16 74193
B04 P27 16 74193
B05 P36 16 74193
B06 P19 14 7430
B07 P45 14 7474
END   0  0
```

INFO MEMORY CONTROL

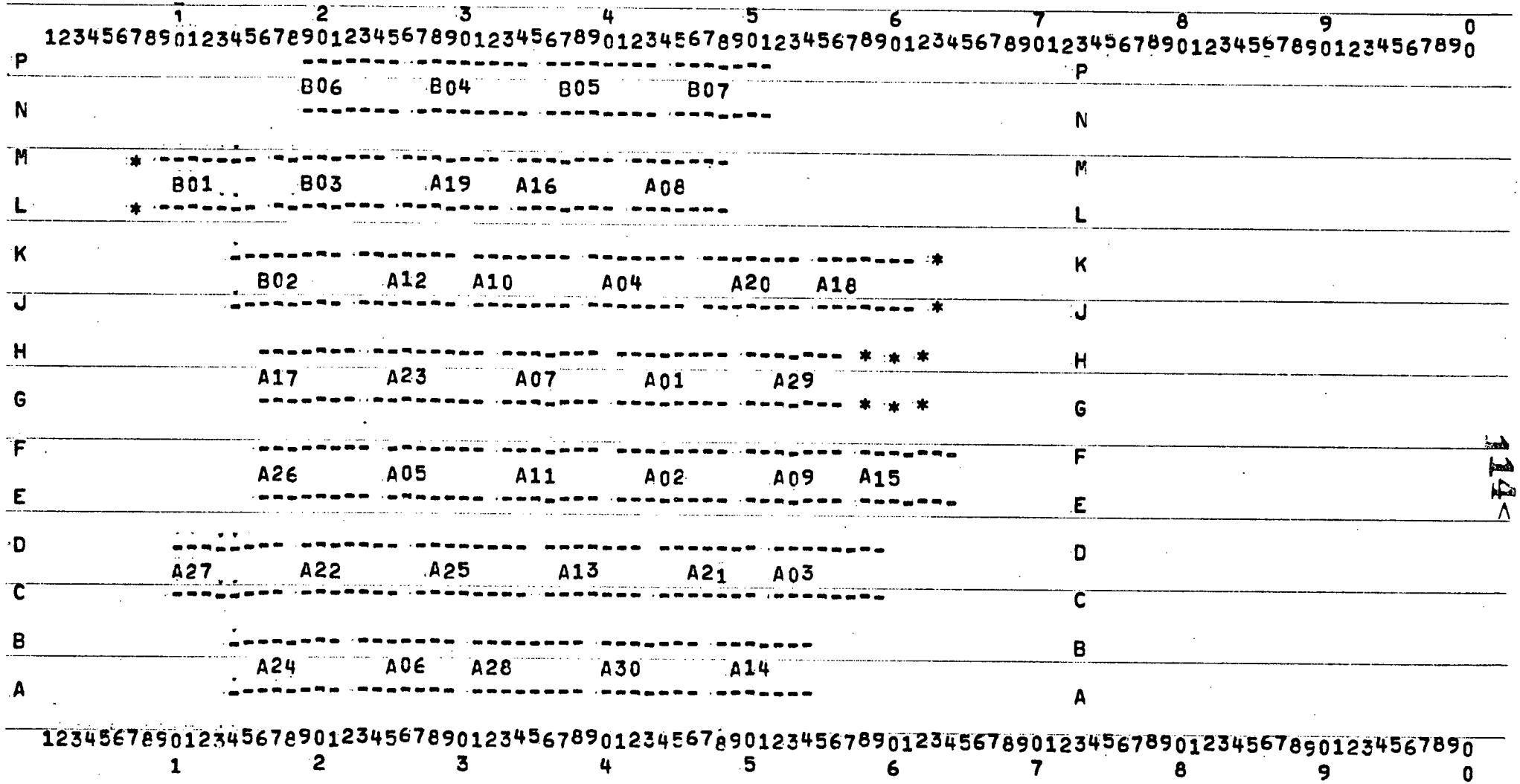
PARTS COUNT — INFO memory control

330	1
5K	1
100PF	1
47PF	1
500PF	1
7475	3
7400	4
7404	1
7408	2
7410	2
7420	1
7432	3
7430	2
74H21	1
7413	1
74H74	4
74H76	1
74163	5
9601	1
74H04	1
74193	4
7474	1

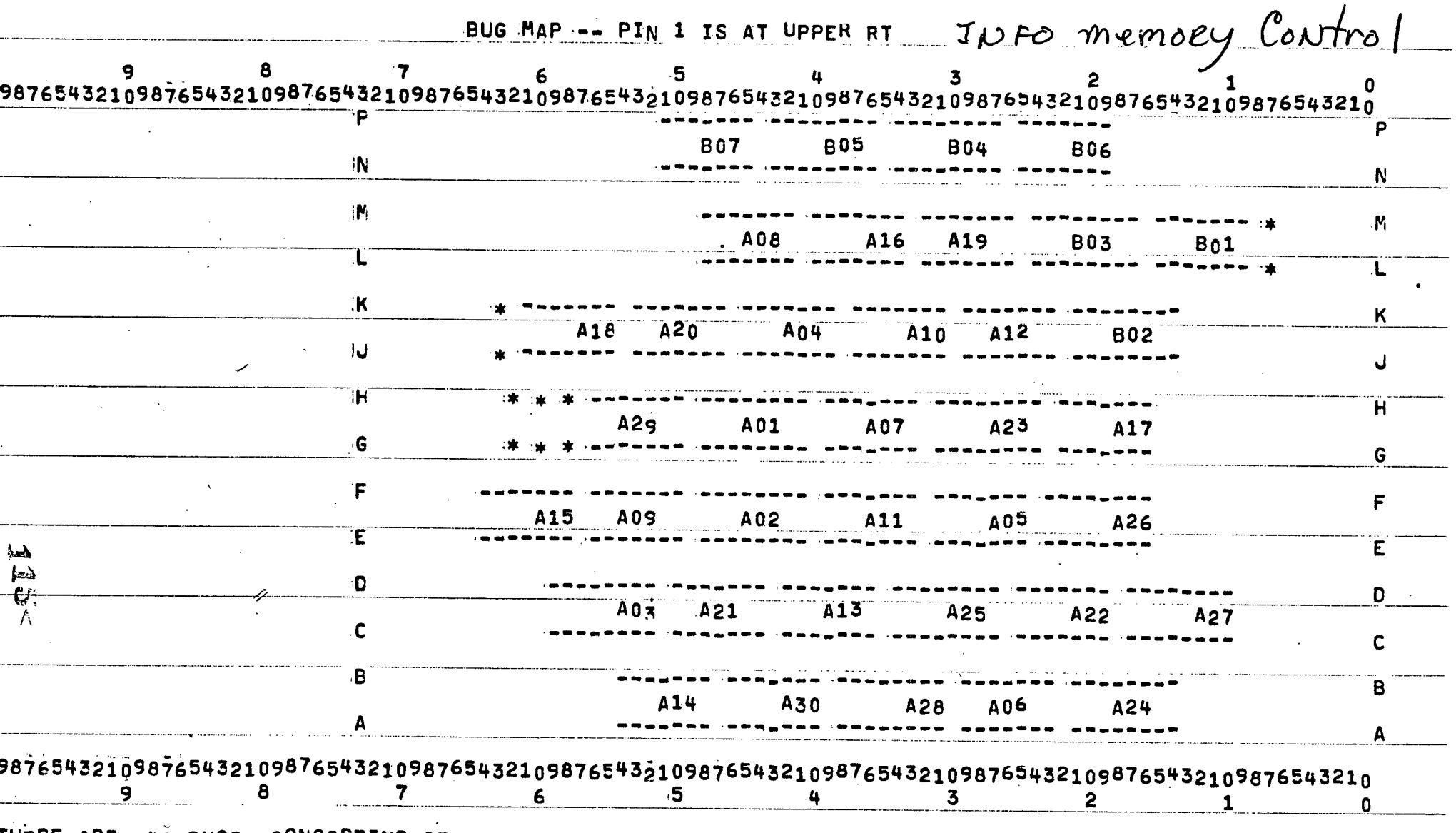
ECN A

Info Memory Control

PIN MAP -- PIN 1 IS AT UPPER LEFT



BUG MAP -- PIN 1 IS AT UPPER RT INFO memory Control

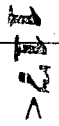


THERE ARE 42 BUGS, CONSISTING OF
0 8-PIN BUGS
24 14-PIN BUGS
13 16-PIN BUGS
0 24-PIN BUGS

BUG	LOC	PINS	ID
A01	B 9	14	74H04
A02	B33	14	74H04
A03	B57	14	74H04
A04	B25	14	7408
A05	P 1	16	74175
A06	P10	16	74175
A07	P37	16	74175
A08	P46	16	74175
A09	H 1	16	74175
A10	H19	16	74175
A11	H37	16	74175
A12	H55	16	74175
A13	P19	16	74175
A14	P28	16	74175
A15	P55	16	74175
A16	P64	16	74175
A17	H10	16	74175
A18	H28	16	74175
A19	H46	16	74175
A20	H64	16	74175
A21	L 6	24	74199
A22	L42	24	74199
A23	L19	24	74199
A24	L55	24	74199
A25	B41	14	74H00
A26	B49	14	7408
B01	D 1	14	7451
B02	D 9	14	7451
B03	F 1	14	7451
B04	F 9	14	7451
B05	D17	14	7451
B06	D25	14	7451
B07	F17	14	7451
B08	F25	14	7451
B09	D41	14	7451
B10	D49	14	7451
B11	F41	14	7451

```
2 F49 14 7451
3 D57 14 7451
4 D65 14 7451
5 F57 14 7451
6 F65 14 7451
7 D33 14 7404
8 F33 14 7404
1 B65 14 102J
2 B17 14 102J
3 B 1 14 102J
D    0  0
```

main memory Buffer

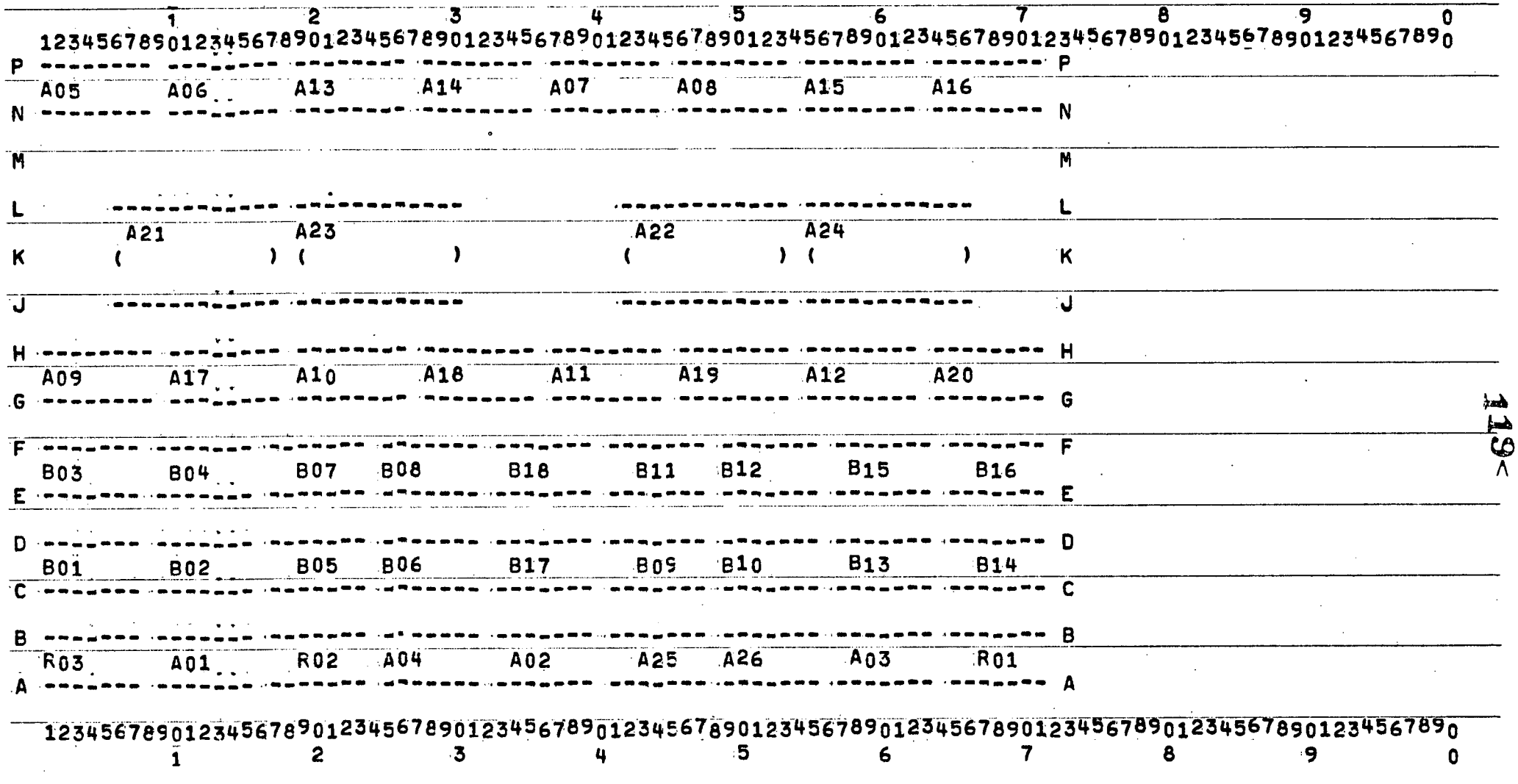


PARTS COUNT main memory Buffer

74H04	3
7408	2
74175	16
74199	4
74H00	1
7451	16
7404	2
102J	3

main memory Buffer

PIN MAP -- PIN 1 IS AT UPPER LEFT



main memory Buffer

BUG MAP -- PIN 1 IS AT UPPER RT

```
          9         8         7         6         5         4         3         2         1         0
9876543210987654321098765432109876543210987654321098765432109876543210987654321098765432109876543210
P ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- P
        A16       A15       A08       A07       A14       A13       A06       A05
N ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- N
M                                                                                         M
L ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- L
                    A24                 A22                 A23                 A21
K         )         ( )         (         )         ( )         (         K
J ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- J
H ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- H
        A20       A12       A19       A11       A18       A10       A17       A09
G ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- G
F ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- F
    B16       B15       B12   B11       B18       B08   B07       B04       B03
E ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- E
D ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- D
    B14       B13       B10   B09       B17       B06   B05       B02       B01
C ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- C
B ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- B
    R01       A03       A26   A25       A02       A04   R02       A01       R03
A ---------- ---------- ---------- ---------- ---------- ---------- ---------- ---------- A
9876543210987654321098765432109876543210987654321098765432109876543210987654321098765432109876543210
          9         8         7         6         5         4         3         2         1         0
```

120 Λ

THERE ARE 47 BUGS, CONSISTING OF
0 8-PIN BUGS
27 14-PIN BUGS
16 16-PIN BUGS
4 24-PIN BUGS

N L 4 - 0 REV ECO 22 AUG 72 PINS-DOWN

BUG	LOC	PINS	ID
A01	T30	0	7402
A02	T46	0	7402
A03	V25	0	7402
A04	R52	16	74161
A05	F47	16	74161
A06	P53	0	74H04
A07	F12	0	7404
A08	H17	0	7400
A09	K 8	0	7400
A10	R27	0	7400
A11	H 9	0	7400
A12	T54	0	7400
A13	T 6	0	7400
A14	T38	0	7404
A15	R35	0	7408
A16	T22	0	7408
A17	R19	0	7410
A18	M 8	0	7420
A19	K16	0	7410
A20	T14	0	7432
A21	V41	0	7402
A22	R 3	0	74H21
A23	V33	0	74H05
A24	R43	16	74H76
A25	P44	16	74H76
A26	D23	16	74H76
A27	V17	0	74H74
A28	P20	0	74S10
A29	M16	0	74S74
A30	P12	0	74S74
A31	R11	0	74S20
A32	K24	0	74S11
A33	P 4	0	7420
A34	V 9	0	MC9601
A35	V49	0	7437
B01	H51	0	7470
B02	M50	0	7470

```
B03 K58 16 74161  Main Memory control for NASD. Sequential
B04 M58 16 74161
B05 H59  0 7400
B06 P61  0 7408
B07 F56  0 7402
B08 D32  0 7400
C01 F20 16 74161
C02 K32 16 74161
C03 F38 16 74161
C04 F29 16 74161
C05 M32 16 74161
C06 H42 16 74161
C07 D40  0 7402
C08 H25 16 7485
C09 M41 16 7485
C10 K49 16 7485
C11 B20 16 74161
C12 B29 16 74175
C13 D14 16 74174
C14 B12  0 7474
C15 P28  0 74H50
C16 M24  0 74H50
C17 K41  0 74H50
C18 H34  0 74H50
C19 P36  0 74H50
C20 H 1  0 74H60
C21 D48  0 74H60
C22 B38  0 74H60
END   0  0
```

PARTS COUNT main memory control for NASA Sequential

7402	6
74161	11
74H04	1
7404	2
7400	8
7408	3
7410	2
7420	2
7432	1
74H21	1
74H05	1
74H76	3
74H74	1
74S10	1
74S74	2
74S20	1
74S11	1
MC9601	1
7437	1
7470	2
7485	3
74175	1
74174	1
7474	1
74H50	5
74H60	3

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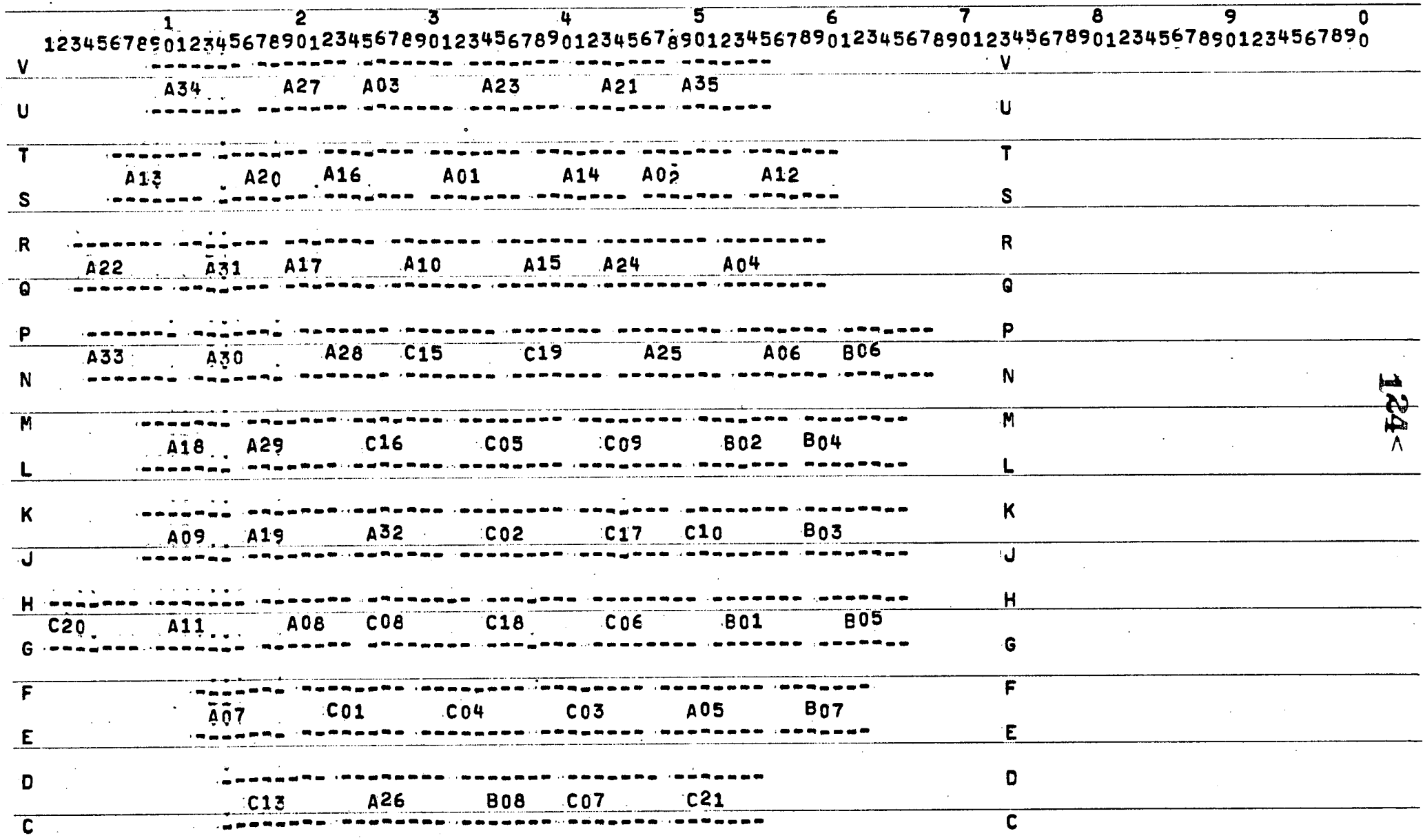
main memory control for NASA Sequential

PIN MAP -- PIN 1 IS AT UPPER LEFT



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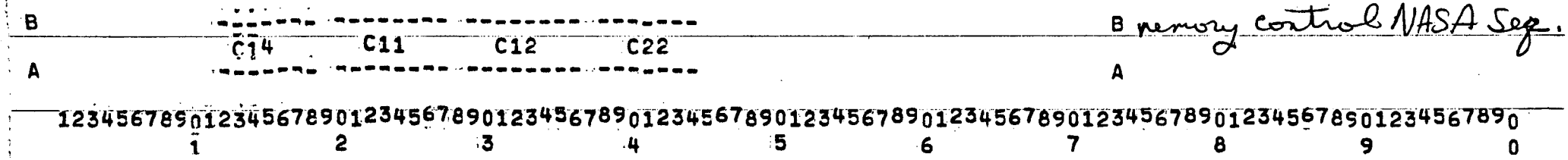
B memory control NASA Seq.



BUG MAP -- PIN 1 IS AT UPPER RT main memory control for NASA Seq.

```
    9 8 7 6 5 4 3 2 1 0
    9876543210987654321098765432109876543210987654321098765432109876543210
V                                                                           V
                        A35     A21       A23       A03   A27       A34
U                                                                           U
T                                                                           T
                    A12     A02   A14       A01       A16   A20       A13
S                                                                           S
R                                                                           R
                        A04     A24   A15       A10       A17   A31       A22
Q                                                                           Q
P                                                                           P
                  B06   A06       A25       C19       C15   A28       A30       A33
N                                                                           N
M                                                                           M
                    B04   B02       C09       C05       C16       A29   A18
L                                                                           L
K                                                                           K
                      B03     C10   C17       C02       A32       A19   A09
J                                                                           J
H                                                                           H
                    B05     B01       C06       C18       C08   A08       A11       C20
G                                                                           G
F                                                                           F
                      B07     A05     C03       C04       C01       A07
E                                                                           E
D                                                                           D
                        C21     C07   B08       A26       C13
C                                                                           C
B                                                                           B
                              C22       C12       C11       C14
```

PUG	LCC	PINS	ID
A01	K23	14	AMS0641
A02	M23	14	AMS0641
A03	P23	14	AMS0641
A04	R23	14	AMS0641
A05	K32	14	AMS0641
A06	M32	14	AMS0641
A07	P32	14	AMS0641
A08	R32	14	AMS0641
A09	T 2	16	10131
A10	P 2	16	10131
A11	H 2	16	10131
A12	D 2	16	10131
A13	D62	16	10131
A14	M62	16	10131
A15	T62	16	10131
A16	D22	16	10131
A17	F32	16	10131
A18	H22	16	10131
A19	H42	16	10131
A20	P42	16	10131
A21	M12	16	10131
A22	D42	16	10131
A23	D12	16	10131
A24	M42	16	10119
A25	R42	16	10119
A26	B62	16	10119
A27	F62	16	10119
A28	K62	16	10119
A29	P62	16	10119
A30	R62	16	10119
A31	V62	16	10119
A32	F52	16	10119
A33	B 2	16	10119
A34	F 2	16	10119
A35	K 2	16	10119
A36	M 2	16	10119
A37	V32	16	10110

127 A

Backup Buffer

```
A38 V42 16 10110
A39 V22 16 10110
A41 V 2 16 10102
A42 R 2 16 10102
A43 V52 16 10109
A44 P52 16 10109
A45 M52 16 10109
A46 H52 16 10109
A47 H32 16 10102
A48 H12 16 10102
A49 D32 16 10111
A50 B22 16 10102
A51 B32 16 10109
A52 K12 16 10111
A53 K52 16 10131
A54 T52 16 10131
A55 D52 16 10131
R56 H62 14 899-1-150
R57 B42 14 899-1-150
R58 F42 14 899-1-150
R59 K42 14 899-1-150
R60 T42 14 899-1-150
R61 F12 14 899-1-150
R62 P12 14 899-1-150
R63 T32 14 899-1-150
R64 T22 14 899-1-150
R65 T12 14 899-1-150
R66 R52 14 899-1-150
R67 B60  2 RC07-91
R68 F60  2 RC07-91
R69 X70  2 RC07-91
R70 H60  2 RC07-91
R71 B10  2 RC07-91
R72 F11  2 RC07-91
R73 K11  2 RC07-91
R74 M11  2 RC07-91
R75 X69  2 RC07-100
R76 X56  2 RC07-100
R77 X67  2 RC07-100
R78 X59  2 RC07-100
R79 M20  2 RC07-100
R80 D30  2 RC07-100
```

Backup Buffer

```
R81 T71   2 RC07-100
R82 D71   2 RC07-100
R83 D60   2 RC07-100
R84 D20   2 RC07-100
R85 P60   2 RC07-100
R86 K60   2 RC07-100
R87 B58   2 RC07-100
R88 K20   2 RC07-100
R89 B12   2 RC07-100
R90 B30   2 RC07-100
R91 B71   2 RC07-100
R92 K71   2 RC07-100
R93 P71   2 RC07-100
R94 B20   2 RC07-100
R95 D10   2 RC07-100
R96 H20   2 RC07-100
R97 B14   2 RC07-100
R98 B16   2 RC07-100
R99 B18   2  OMIT
END   0   0
```

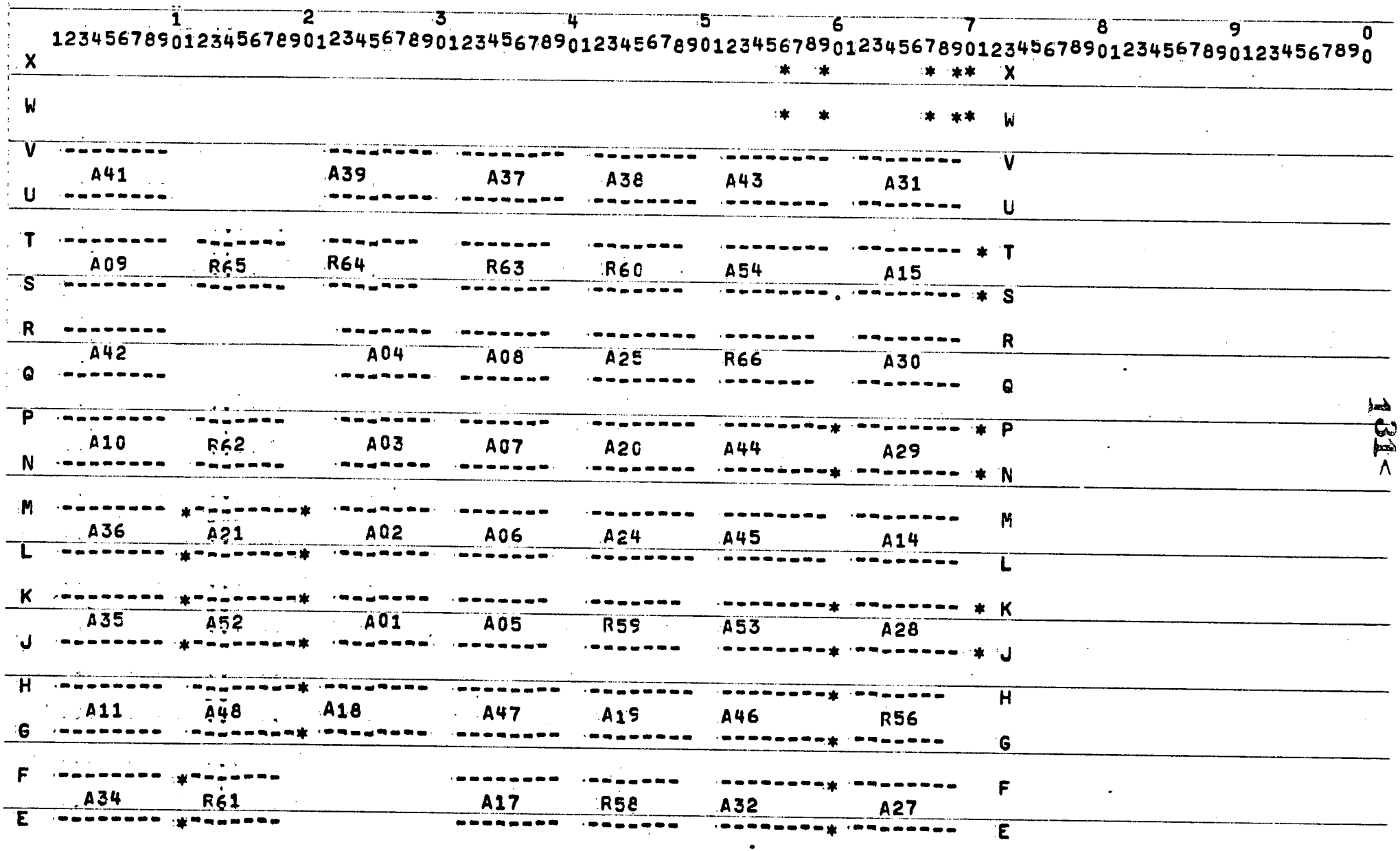
129A

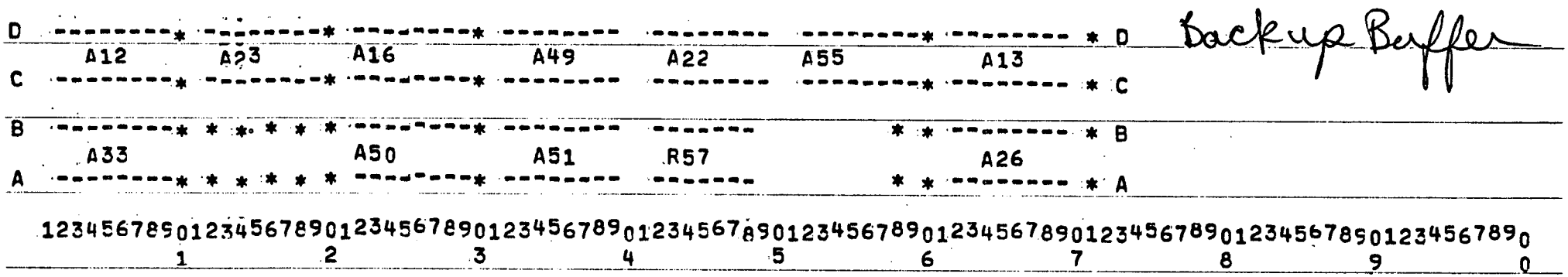
PARTS COUNT Back up Buffer

AMS0641	8
10131	18
10119	13
10110	3
10102	5
10109	5
10111	2
899-1-150	11
RC07-91	8
RC07-100	24
OMIT	1

Backup Buffer

PIN MAP -- PIN 1 IS AT UPPER LEFT



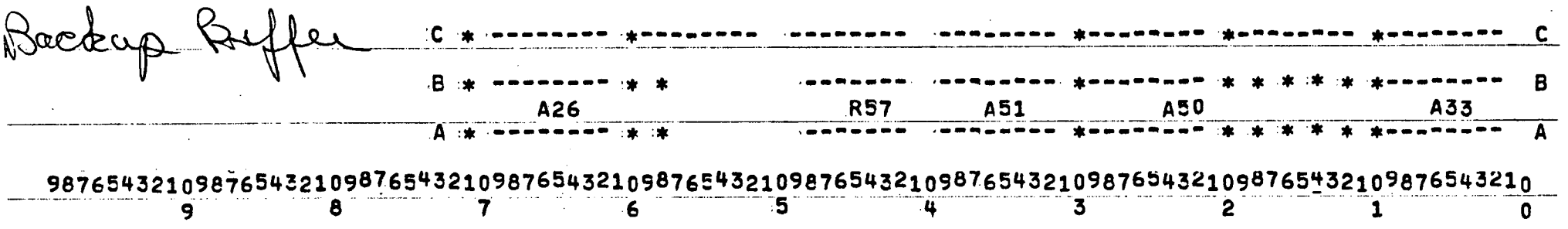


Backup Buffer

BUG MAP -- PIN 1 IS AT UPPER RT Back up Buffer

```
    9         8         7         6         5         4         3         2         1         0
9876543210987654321098765432109876543210987654321098765432109876543210987654321098765432109876543210
X  ** *       * *                                                                               X
W  ** *       * *                                                                               W
V  -------- -------- -------- -------- --------                                   --------       V
      A31       A43       A38      A37       A39                                    A41
U  -------- -------- -------- -------- --------                                   --------       U
T *-------- -------- -------- -------- -------- -------- --------                              T
      A15       A54       R60      R63       R64      R65      A09
S *-------- -------- -------- -------- -------- -------- --------                              S
R  -------- -------- -------- -------- --------                                   --------       R
      A30       R66       A25      A08       A04                                    A42
Q  -------- -------- -------- -------- --------                                   --------       Q
P *-------- *------- -------- -------- -------- -------- --------                              P
      A29       A44       A20      A07       A03      R62      A10
N *-------- *------- -------- -------- -------- -------- --------                              N
M  -------- -------- -------- -------- --------  *------*  --------                           M
      A14       A45       A24      A06       A02      A21      A36
L  -------- -------- -------- -------- --------  *------*  --------                           L
K *-------- *------- -------- -------- --------  *------*  --------                           K
      A28       A53       R59      A05       A01      A52      A35
J *-------- *------- -------- -------- --------  *------*  --------                           J
H  -------- *------- -------- -------- --------  *------- --------                           H
      R56       A46       A19      A47       A18      A48      A11
G  -------- *------- -------- -------- --------  *------- --------                           G
F  -------- *------- -------- --------                    -------- --------                  F
      A27       A32       R58      A17                    R61      A34
E  -------- *------- -------- --------                    -------- --------                  E
D *-------- *------- -------- -------- --------  *------- --------                           D
      A13       A55       A22      A49       A16      A23      A12
```

Backup Buffer



THERE ARE 98 BUGS, CONSISTING OF
0 8-PIN BUGS
19 14-PIN BUGS
46 16-PIN BUGS
0 24-PIN BUGS

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BUG	LOC	PINS	ID
A01	B62	16	10131
A02	V62	16	10131
A03	R62	16	10131
A04	H62	16	10131
A05	D62	16	10131
A06	V52	16	10131
A07	F42	16	10131
A08	M42	16	10131
A09	T42	16	10131
A10	R22	16	10131
A11	K22	16	10131
A12	D22	16	10131
A13	K 2	16	10131
A14	R 2	16	10131
A15	D 2	16	10131
A16	P62	16	10102
A17	M62	16	10102
A18	K62	16	10102
A19	F62	16	10102
A20	D52	16	10102
A21	B42	16	10109
A22	D42	16	10109
A23	H42	16	10102
A24	K42	16	10102
A25	P42	16	10102
A26	R42	16	10102
A27	T22	16	10102
A28	P22	16	10102
A29	M22	16	10102
A30	H22	16	10102
A31	T 2	16	10102
A32	P 2	16	10102
A33	M 2	16	10102
A34	B22	16	10102
A35	B 2	16	10102
A36	H 2	16	10102

Syndrome Corrector 1

```
37 F22 16 10102
38 V32 16 10110
39 V22 16 10110
40 V12 16 10110
41 V42 16 10110
42 F 2 16 10102
43 P52 14 899-1-R150
44 F52 14 899-1-R150
45 R32 14 899-1-R150
46 K32 14 899-1-R150
47 D32 14 899-1-R150
48 R12 14 899-1-R150
49 K12 14 899-1-R150
50 F12 14 899-1-R150
51 X64  2 RC07-47
52 X63  2 RC07-100
53 T58  2 RC07-51
54 B38  2 RC07-100
55 B37  2 RC07-47
56 D13  2
57 R71  2
58 B71  2
59 H52  2
60 F32  2
61 H12  2
62 H54  2
63 K71  2
64 M71  2
65 B52  2
66 B12  2
67 B18  2
68 H32  2
69 F71  2
70 H71  2
71 H34  2
72 B16  2
73 B14  2
74 B32  2
75 B35  2
76 B54  2
77 B34  2
78 D14  2
```

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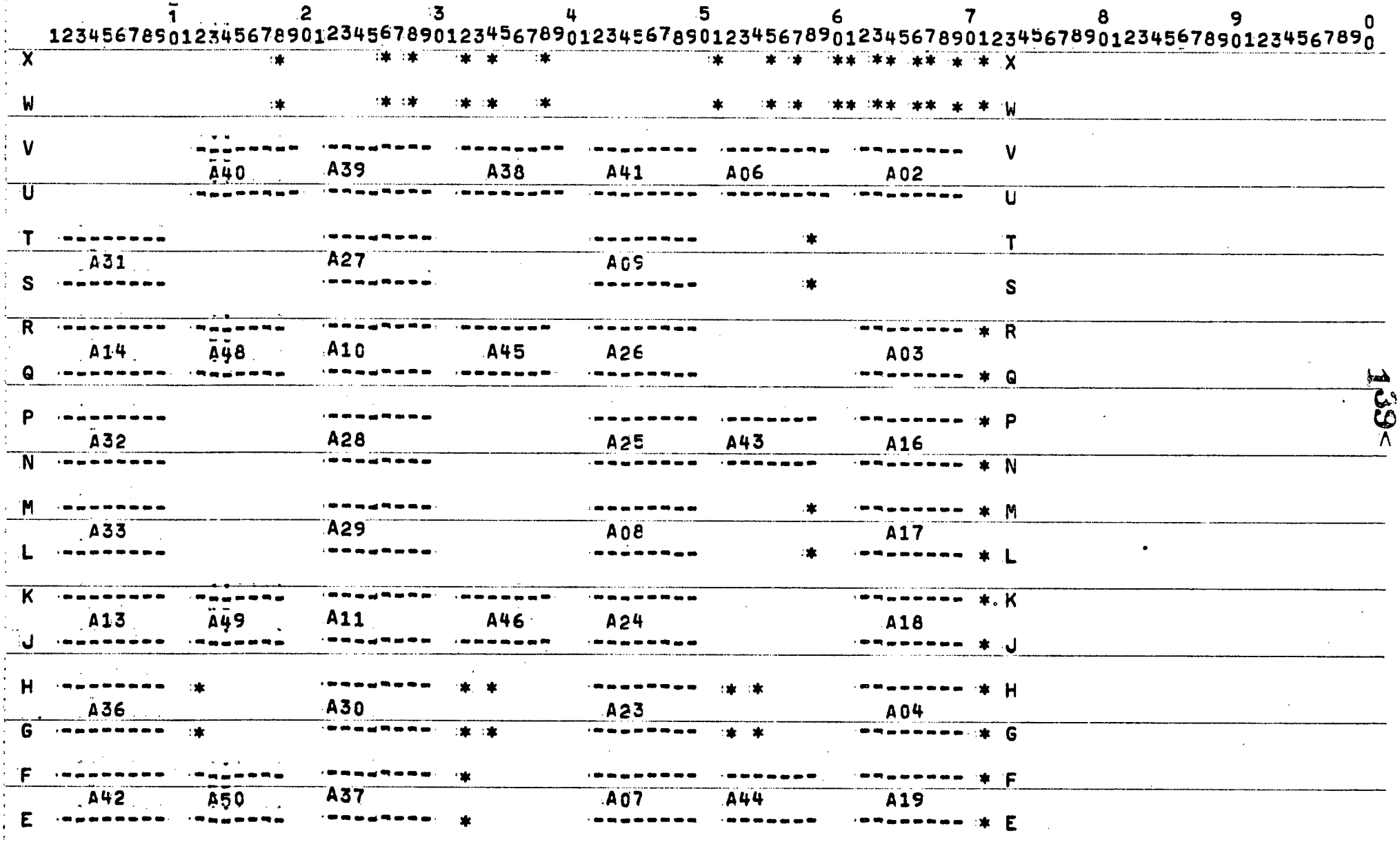
```
A79 X38  2      SYNDROME CORRECTOR1
A80 X28  2
A81 X18  2
A82 X26  2
A83 X32  2
A84 X34  2
A85 X67  2
A86 X69  2
A87 X71  2
A88 X66  2
A89 P71  2
A90 B59  2
A91 B58  2
A92 B57  2
A93 B56  2
A94 X61  2
A95 X60  2
A96 M58  2
A97 X51  2
A98 X55  2
A99 X57  2
END   0  0
```

PARTS COUNT SYNDROME CORRECTOR 1

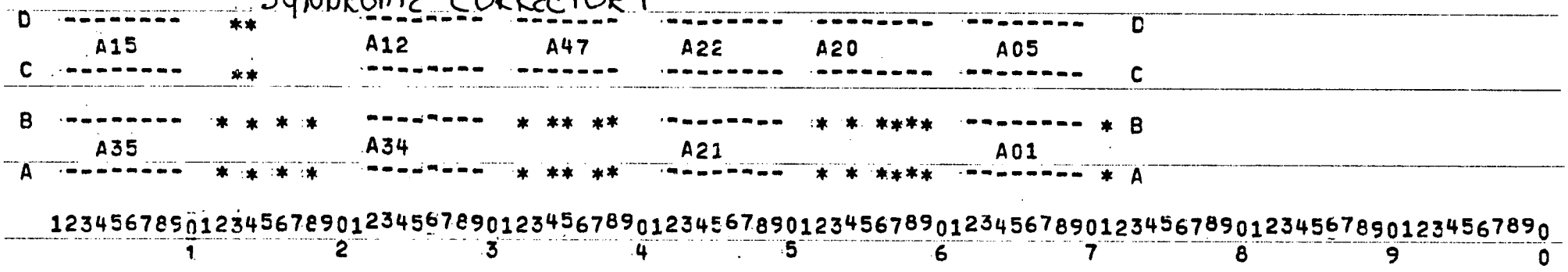
10131	15
10102	21
10109	2
10110	4
899-1-R150	8
RC07-47	2
RC07-100	2
RC07-51	1
	44

SYNDROME CORRECTOR 1

PIN MAP -- PIN 1 IS AT UPPER LEFT

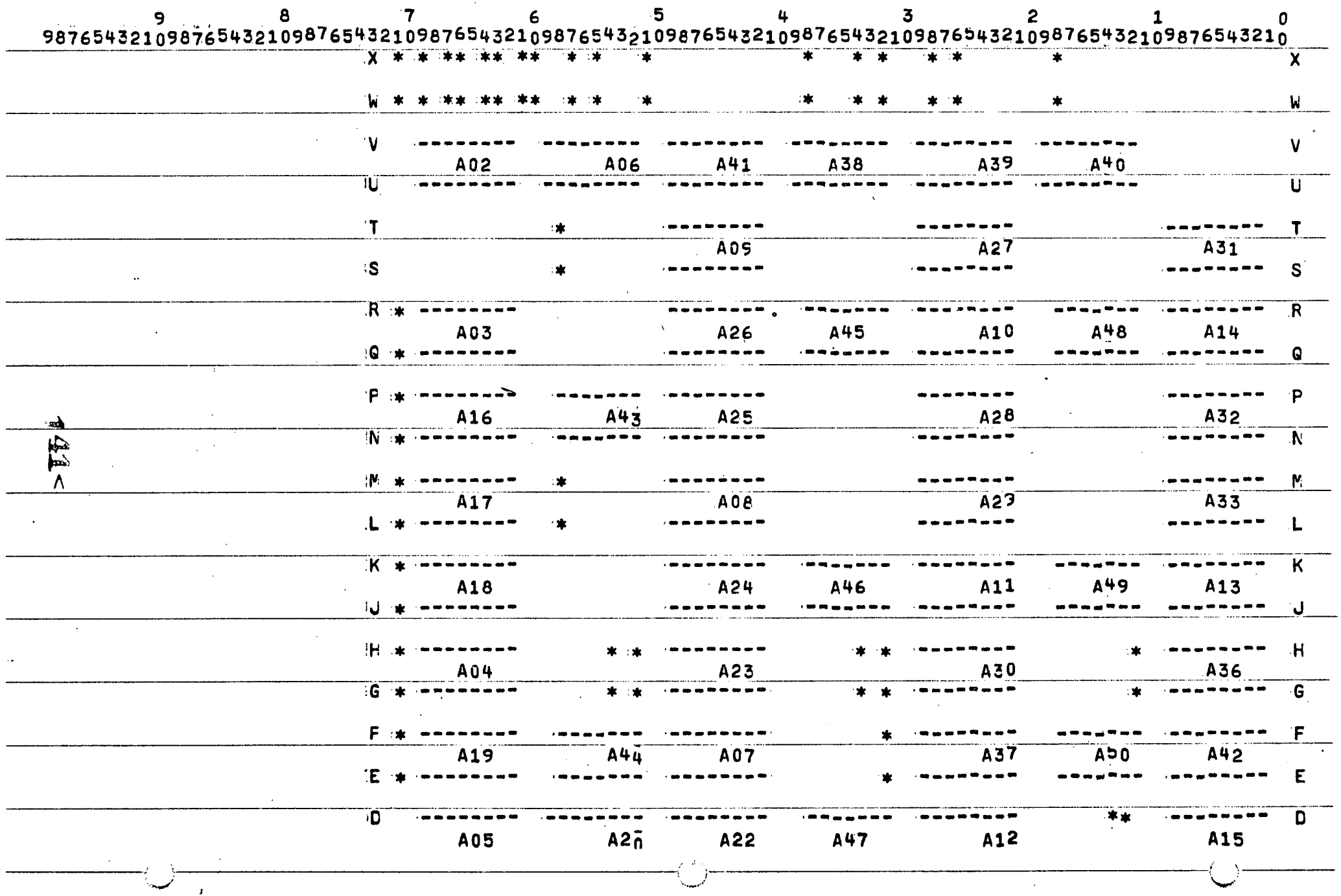


Syndrome Corrector I

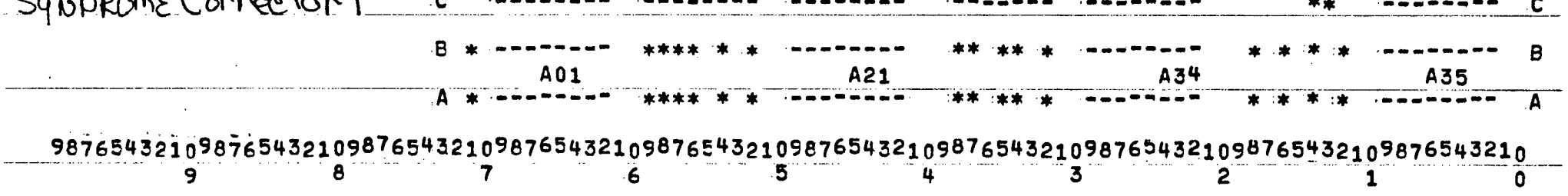


Syndrome Corrector I

BUG MAP -- PIN 1 IS AT UPPER RT



Syndrome Corrector I



THERE ARE 99 BUGS, CONSISTING OF
0 8-PIN BUGS
8 14-PIN BUGS
42 16-PIN BUGS
0 24-PIN BUGS

27

SYNDROME CORRECTOR 2 JOB 6000

W L - 1 0 REV ECO 22 AUG 72 PINS-DOWN

BUG	LOC	PINS	ID
A01	D 2	16	10131
A02	K 2	16	10131
A03	P 2	16	10131
A04	P22	16	10131
A05	K22	16	10131
A06	B22	16	10131
A07	H42	16	10131
A08	P42	16	10131
A09	P62	16	10131
A10	H62	16	10131
A11	F 2	16	10102
A12	H 2	16	10102
A13	M 2	16	10102
A14	R 2	16	10102
A15	R22	16	10102
A16	M22	16	10102
A17	H22	16	10102
A18	D42	16	10109
A19	F22	16	10109
A20	D22	16	10109
A21	B42	16	10102
A22	F42	16	10102
A23	K42	16	10102
A24	M42	16	10102
A25	R42	16	10102
A26	R62	16	10102
A27	M62	16	10102
A28	K62	16	10102
A29	B62	16	10109
A30	D62	16	10109
A31	F62	16	10109
A32	T46	16	10110
A33	T36	16	10110
A34	T26	16	10110
A35	T16	16	10110
R36	M52	14	899-1-150
R37	F52	14	899-1-150

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Syndrome connector 2.

```
38 M32 14 e99-1-150
39 F32 14 e99-1-150
40 M12 14 e99-1-150
41 F12 14 e99-1-150
42 B 8  2 125MW-47
43 B 6  2 125MW-100
44 B10  2 CMIT
45 B56  2 125MW-100
46 B54  2 125MW-47
75 B60  2 CMIT
76 B58  2 CMIT
77 D56  2 125MW-4.7K
51 V52  2 CMIT
70 V28  2 CMIT
71 V36  2 CMIT
72 V32  2 CMIT
73 V30  2 CMIT
74 V34  2 CMIT
47 H52  2 125MW-51
48 H71  2 125MW-51
49 B32  2 125MW-51
50 D12  2 125MW-51
52 D14  2 125MW-51
53 B40  2 125MW-51
54 M71  2 125MW-51
55 D60  2 125MW-51
56 D50  2 125MW-51
57 D16  2 125MW-51
58 K12  2 125MW-51
59 D32  2 125MW-51
60 H40  2 125MW-51
61 H54  2 125MW-51
62 D34  2 125MW-51
03 B50  2
02 B71  2
01 D54  2
69 B38  2 125MW-51
68 D40  2 125MW-51
67 D71  2 125MW-51
66 B52  2 125MW-51
65 D52  2 125MW-51
64 P32  2 125MW-51
```

```
R63 K14   2 125MW-51      SYNDROME CORRECTOR 2
C04 B36   2
C05 B12   2
C06 D58   2
C07 D36   2
C08 D18   2
C09 F71   2
C10 F50   2
C11 F30   2
C12 F10   2
C13 H50   2
C14 K71   2
C15 K10   2
C16 M50   2
C17 M30   2
C18 M10   2
C19 P71   2
C20 P34   2
C21 V54   2
C22 V38   2
END   0   0
```

PARTS COUNT Syndrome Corrector 2

10131	10
10102	15
10109	6
10110	4
899-1-150	6
125MW-47	2
125MW-100	2
OMIT	9
125MW-4.7K	1
125MW-51	22
	22

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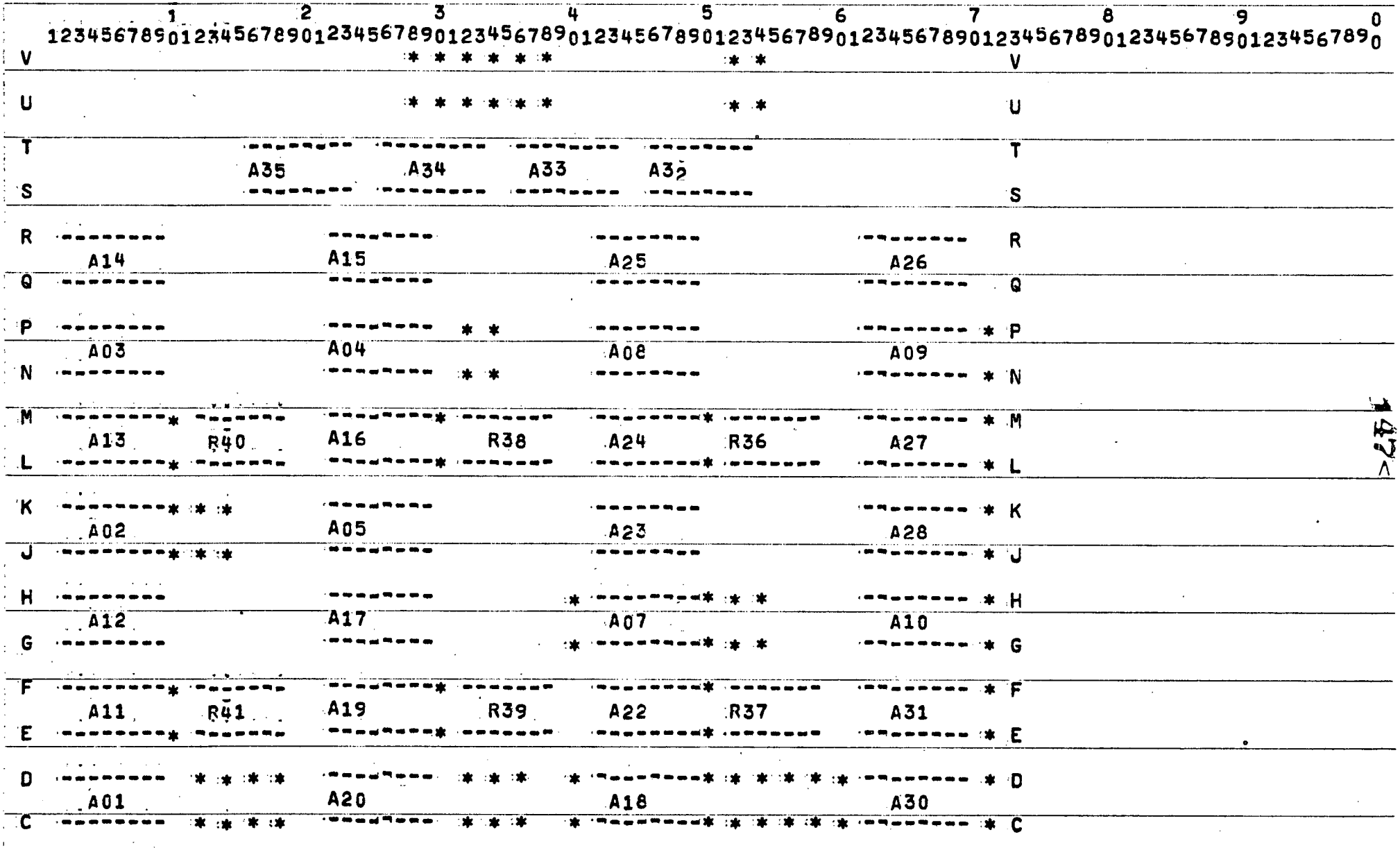
Syndrome Corrector 2

PIN MAP -- PIN 1 IS AT UPPER LEFT

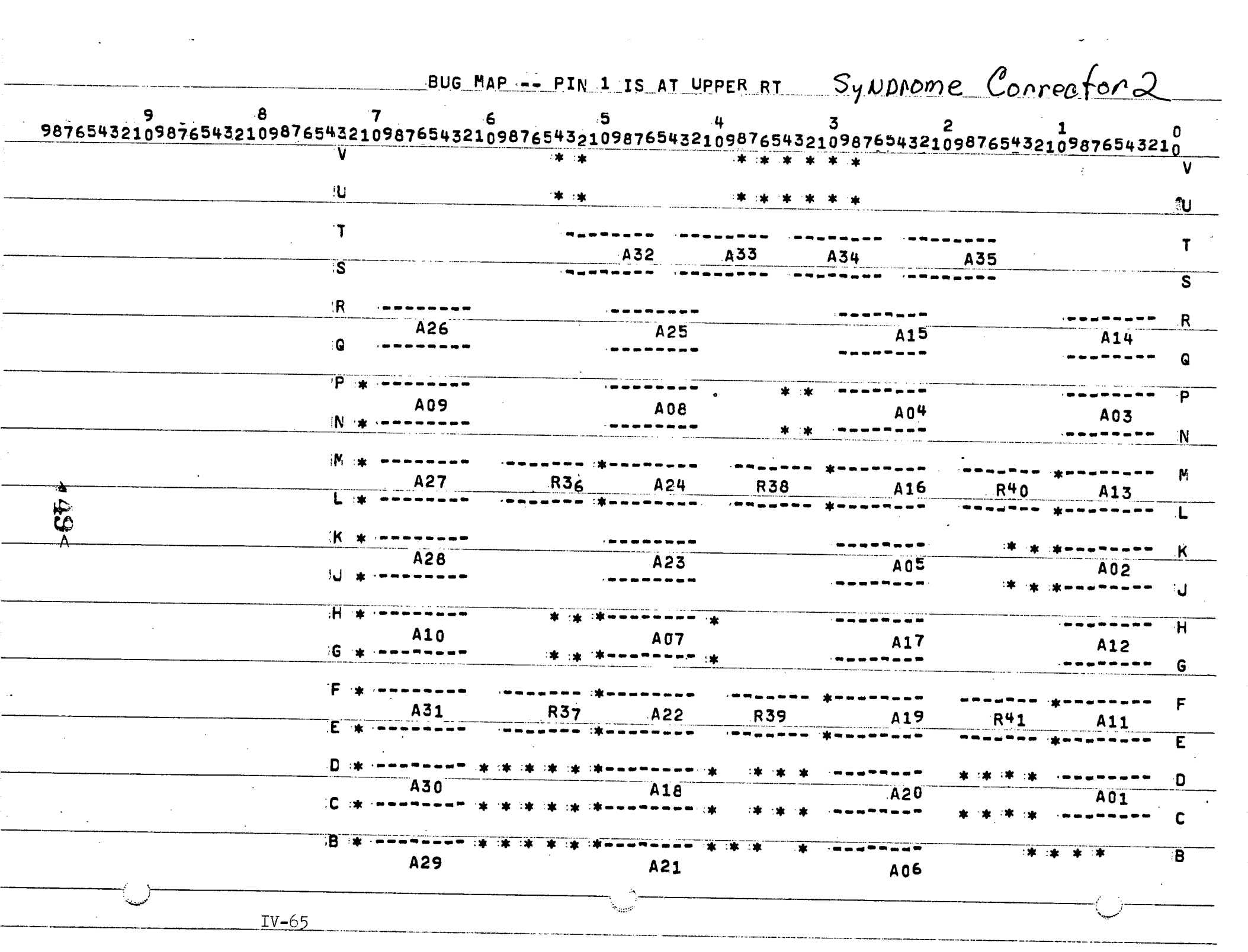


```
B     * * * *          ---------  *  * * * ---------* * * * * --------  * B
                       A06                  A21                  A29
A     * * * *          ---------  *  * * * ---------* * * * * --------  * A

12345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
          1         2         3         4         5         6         7         8         9         0
```

Syndrome Corrector 2

BUG MAP -- PIN 1 IS AT UPPER RT Syndrome Correct for 2



BUG	LOC	PINS	ID
A01	H32	16	10131
A02	H22	16	10131
A03	H12	16	10131
A04	H 2	16	10131
A05	F32	16	10131
A06	F22	16	10131
A07	F12	16	10131
A08	F 2	16	10131
A09	M 2	16	10131
A10	M22	16	10131
A11	M32	16	10131
A12	R12	16	10131
A13	R32	16	10131
A14	R52	16	10131
A15	P22	16	10131
A16	P52	16	10131
A17	H62	16	10131
A18	F62	16	10131
A19	T52	16	10131
A20	D32	16	10102
A21	D22	16	10102
A22	D12	16	10102
A23	D 2	16	10102
A24	D42	16	1039
A25	D52	16	1039
A26	B46	16	1039
A28	R 2	16	10119
A29	R22	16	10119
A30	R42	16	10102
A31	R62	16	10102
A32	P12	16	10109
A33	P62	16	10109
A34	T32	16	10109
A35	T22	16	10109
A36	P42	16	10109
A37	V12	16	10109
A38	M12	16	10109

Backsearch Counter & Interface BD

```
A 39 D62 16 10110
A 40 V22 16 10110
A 41 H52 16 10109
A 42 V32 16 10110
A 43 H42 16 10110
R 01 B36 10 TERM
R 02 B31 10 TERM
R 03 B26 10 TERM
R 04 B21 10 TERM
R 05 B16 10 TERM
R 06 B11 10 TERM
R 07 B 6 10 TERM
R 08 B 1 10 TERM
R 09 B55 10 TERM
R 42 K 2 14 899-1-150
R 43 K12 14 899-1-150
R 44 K22 14 899-1-150
R 45 K32 14 899-1-150
R 48 T12 14 899-1-150
R 49 T42 14 899-1-150
R 51 F42 14 899-1-150
R 52 F52 14 899-1-150
R 53 M62 14 899-1-150
R 55 B41  2 RC07-100
R 56 B42  2 RC07-100
R 57 B43  2 RC07-100
R 58 B44  2 RC07-100
R 59 B60  2 RC07-100
R 60 B61  2 RC07-100
R 61 X34  2 RC07-100
R 62 X35  2 RC07-100
R 63 X36  2 RC07-100
R 64 X37  2 RC07-100
R 65 B62  2 RC07-100
R 66 B63  2 RC07-100
R 67 B64  2 RC07-100
R 68 B65  2 RC07-100
R 69 B67  2 RC07-100
R 70 B68  2 RC07-100
R 71 B69  2 RC07-100
R 72 B70  2 RC07-100
R 75 X39  2 RC07-100
```

Back Search Counter and Interface BD

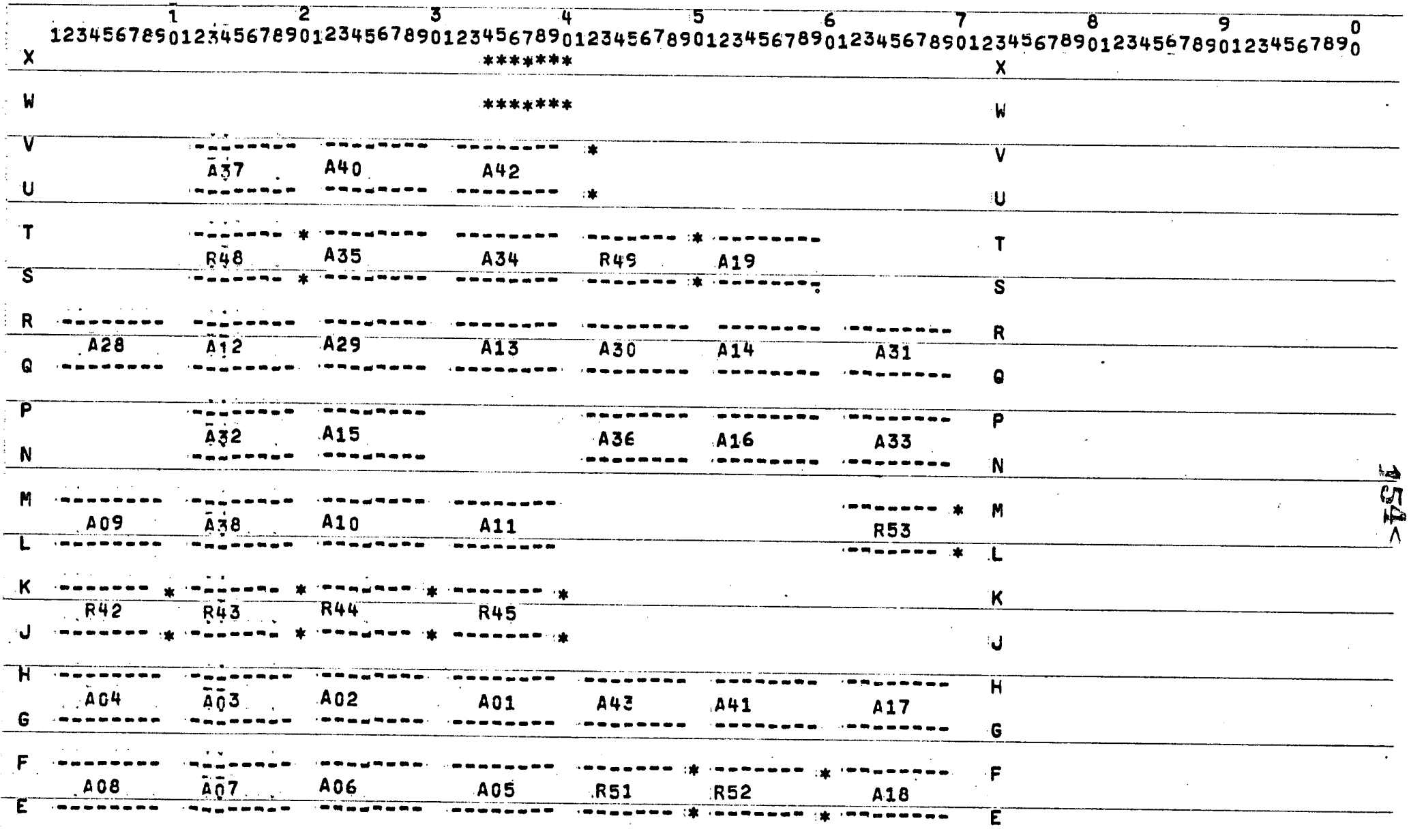
R76	X40	2	RC07-100
R77	V42	2	RC07-150
C01	B71	2	
C02	B66	2	
C03	K10	2	
C04	K20	2	
C05	K30	2	
C06	K40	2	
C07	T20	2	
C08	T50	2	
C09	F50	2	
C10	F60	2	
C11	M70	2	
C12	B45	2	
C13	X38	2	
END	0	0	

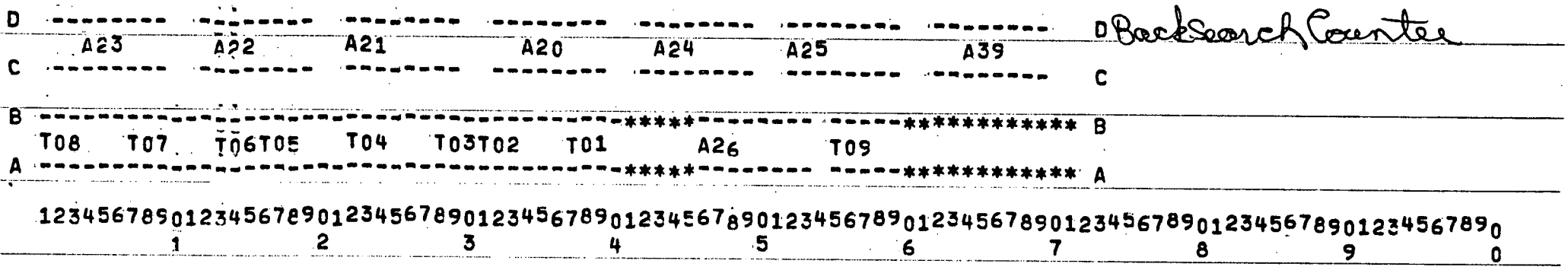
PARTS FOUNT Backsearch Counter and Interface B.D.

10131	19
10102	6
1039	3
10119	2
10109	8
10110	4
TERM	9
899-1-150	9
RC07-100	20
RC07-150	1
	13

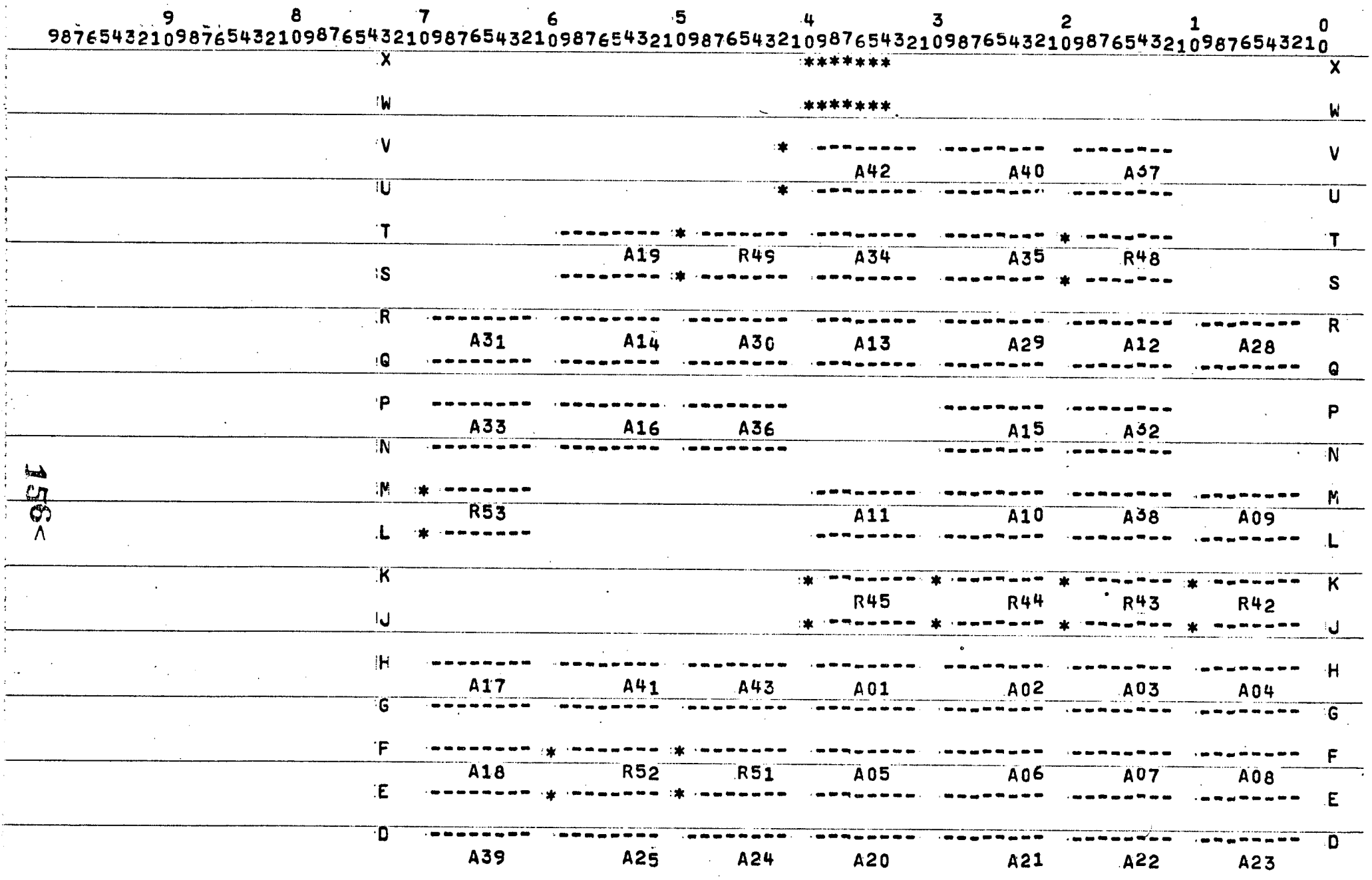
Backsearch Counter & Interface BD

PIN MAP -- PIN 1 IS AT UPPER LEFT




D
A23
A22
A21
A20
A24
A25
A39
D Backsearch Counter
C
C
B
T08
T07
T06
T05
T04
T03
T02
T01
A26
T09
B
A
A
1234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890
1
2
3
4
5
6
7
8
9
0

BUG MAP -- PIN 1 IS AT UPPER RT Backsearch Counter



sacksearch Counter

```
C --------  --------  --------  --------  --------  --------  --------  -------- C
B ********** ---------- ********** ---------- ********** ---------- ********** -------- B
                  T09       A26       T01    T02T03    T04    T05T06    T07    T08
A ********** ---------- ********** ---------- ********** ---------- ********** -------- A

9876543210987654321098765432109876543210987654321098765432109876543210987654321098765432109876543210
          9         8         7         6         5         4         3         2         1         0
```

THERE ARE 94 BUGS, CONSISTING OF
- 0 8-PIN BUGS
- 9 14-PIN BUGS
- 42 16-PIN BUGS
- 0 24-PIN BUGS

BACKPLANE PART-1

CFCLK
P 90
G 73
G 74

SLCF
P 91
F 94
H 94
K 94
M 94

ICCLK
P 86
E 64

SLIF
P 88
F 75
H 75
K 75
M 75

CFUNT
P 74

RCPCF
P 16
F 86
H 86
K 86
M 86

OVACNT
P 75
G 71
G 72

CFOVT
P 72
G 77
G 78

SRCL
P 90
F 92
H 92
K 92
M 92

CFWG
P 38
F 50

ICWG
P 22
F 51
H 51
K 51
M 51

WCPCA
P 44
K 95
M 95

WCPCB
P 66
F 95
H 95

SCPC
F 61
F 69
H 69
K 69
M 69

MCLKF
P 58
G 94
J 94
L 94
N 94

RCPIF
P 3
F 89
H 89
K 89
M 89

WCPIA
P 45
K 96
M 96

WCPIB
P 67
F 96

H 96

SCPI

P 59
F 74
H 74
K 74
M 74

RESF

F 8
G 12
J 12
L 12
N 12

ERROR

P 96

MA0F

P 14
G 10
J 10
L 10
N 10

MA1F

P 15
G 14
J 14
L 14
N 14

MA2F

F 12
G 16
J 16
L 16
N 16

MA3F

P 13
G 20
J 20
L 20
N 20

MA4F

P 17
G 18

J 18
L 18
N 18

MA5F

P 10
G 86
J 86
L 86
N 86

MA6F

P 42
G 84
J 84
L 84
N 84

MA7F

P 43
G 96
J 96
L 96
N 96

MA8F

P 46
G 88
J 88
L 88
N 88

MA9F

P 47
G 92
J 92
L 92
N 92

MCT

P 48

SAS1

P 82

SAS2

P 83

SAS3

P 80

SAS4

P 81

MC3B

P 27
E 40

MC4B

P 49
E 56

MC5B

P 50
E 41

MC6B

P 52
E 48

MC7B

P 51
E 80

MC8B

P 63
E 49

MC9B

P 64
E 81

AW00T

F 3
G 95

AW00F

F 4
G 89

AW01T

F 5
G 85

AW01F

F 6
G 77

AW02T

F 7
G 75

AW02F

F 8
G 65

AW03T

F 9

G 63

AW03F

F 10

G 51

AW04T

F 18

G 45

AW04F

F 19

G 37

AW05T

F 34

G 35

AW05F

F 35

G 23

AW06T

F 16

G 21

AW06F

F 17

G 11

AW07T

F 32

G 9

AW07F

F 33

G 6

AW08T

F 66

G 90

AW08F

F 67

G 97

AW09T

F 82

G 81

AW09F

F 83

G 83

AW10T

F 64

G 69

AW10F

F 65
G 71

AW11T

F 80
G 57

AW11F

F 81
G 59

AW12T

F 87
G 39

AW12F

F 84
G 43

AW13T

F 85
G 27

AW13F

F 78
G 29

AW14T

F 79
G 15

AW14F

F 76
G 17

AW15T

F 77
G 4

AW15F

F 72
G 7

AS00

F 11
G 93

AS01

F 12
G 87

AS02

F 13

```
          G 73
AS03
          F 14
          G 61
AS04
          F 15
          G 53
AS05
          F 20
          G 33
AS06
          F 48
          G 19
AS07
          F 49
          G  5
AS08
          F 52
          G 91
AS09
          F 53
          G 79
AS10
          F 46
          G 67
AS11
          F 47
          G 55
AS12
          F 93
          G 41
AS13
          F 90
          G 25
AS14
          F 91
          G 13
AS15
          F 88
          G  3
BAITI
          F 36
```

BA0TI
F 73
B30TC
F 71
G 23
G 24
B3ITC
F 30
G 85
G 86
B70TC
F 70
G 13
G 14
B7ITC
F 37
G 59
G 60
BW00T
H 3
J 95
BW00F
H 4
J 89
BW01T
H 5
J 85
BW01F
H 6
J 77
BW02T
H 7
J 75
BW02F
H 8
J 65
BW03T
H 9
J 63
BW03F
H 10
J 51

Bk04T	H	18
	J	45
Bk04F	H	19
	J	37
Bk05T	H	34
	J	35
BW05F	H	35
	J	23
BW06T	H	16
	J	21
BW06F	H	17
	J	11
BW07T	H	32
	J	9
BW07F	H	33
	J	6
BW08T	H	66
	J	90
BW08F	H	67
	J	97
BW09T	H	82
	J	81
BW09F	H	83
	J	83
BW10T	H	64
	J	69
BW10F	H	65
	J	71

BW11T
H 80
J 57

BW11F
H 81
J 59

BW12T
H 87
J 39

BW12F
H 84
J 43

BW13T
H 85
J 27

BW13F
H 78
J 29

BW14T
H 79
J 15

BW14F
H 76
J 17

BW15T
H 77
J 4

BW15F
H 72
J 7

BS00
H 11
J 93

BS01
H 12
J 87

BS02
H 13
J 73

BS03
H 14
J 61

BS04
H 15
J 53
BS05
H 20
J 33
BS06
H 48
J 19
BS07
H 49
J 5
BS08
H 52
J 91
BS09
H 53
J 79
BS10
H 46
J 67
BS11
H 47
J 55
BS12
H 93
J 41
BS13
H 90
J 25
BS14
H 91
J 13
BS15
H 88
J 3
BBITI
H 36
BBOTI
H 73
B20TC
H 71

169

```
                G 27
                G 28
B2ITC
                H 30
                G 79
                G 80
B6OTC
                H 70
                G 11
                G 12
B6ITC
                H 37
                G 69
                G 70
CW00T
                K  3
                L 95
CW00F
                K  4
                L 89
CW01T
                K  5
                L 85
CW01F
                K  6
                L 77
CW02T
                K  7
                L 75
CW02F
                K  8
                L 65
CW03T
                K  9
                L 63
CW03F
                K 10
                L 51
CW04T
                K 18
                L 45
CW04F
```

Add

	K 19
	L 37
CW05T	
	K 34
	L 35
CW05F	
	K 35
	L 23
CW06T	
	K 16
	L 21
CW06F	
	K 17
	L 11
CW07T	
	K 32
	L 9
CW07F	
	K 33
	L 6
CW08T	
	K 66
	L 90
CW08F	
	K 67
	L 97
CW09T	
	K 82
	L 81
CW09F	
	K 83
	L 83
CW10T	
	K 64
	L 69
CW10F	
	K 65
	L 71
CW11T	
	K 80
	L 57
CW11F	

TABLE A

K 81
L 59

CW12T

K 87
L 39

CW12F

K 84
L 43

CW13T

K 85
L 27

CW13F

K 78
L 29

CW14T

K 79
L 15

CW14F

K 76
L 17

CW15T

K 77
L 4

CW15F

K 72
L 7

CS00

K 11
L 93

CS01

K 12
L 87

CS02

K 13
L 73

CS03

K 14
L 61

CS04

K 15
L 53

CS05

K 20
L 33

CS06

K 48
L 19

CS07

K 49
L 5

CS08

K 52
L 91

CS09

K 53
L 79

CS10

K 46
L 67

CS11

K 47
L 55

CS12

K 93
L 41

CS13

K 90
L 25

CS14

K 91
L 13

CS15

K 88
L 3

BCITI

K 36

BCOTI

K 73

B1OTC

K 71
Q 43
Q 44

B1ITC

K 30

```
                G 81
                G 82
        B50TC
                K 70
                G  9
                G 10
        B5ITC
                K 37
                G 55
                G 56
        Dh00T
                M  3
                N 95
        Dh00F
                M  4
                N 89
        Dh01T
                M  5
                N 85
        Dh01F
                M  6
                N 77
        Dh02T
                M  7
                N 75
        Dh02F
                M  8
                N 65
        Dh03T
                M  9
                N 63
        Dh03F
                M 10
                N 51
        Dh04T
                M 18
                N 45
        Dh04F
                M 19
                N 37
        Dh05T
                M 34
```

N 35

DW05F

M 35
N 23

DW06T

M 16
N 21

DW06F

M 17
N 11

DW07T

M 32
N 9

DW07F

M 33
N 6

DW08T

M 66
N 90

DW08F

M 67
N 97

DW09T

M 82
N 81

DW09F

M 83
N 83

DW10T

M 64
N 69

DW10F

M 65
N 71

DW11T

M 80
N 57

DW11F

M 81
N 59

DW12T

M 87

```
          N 39
DW12F
          M 84
          N 43
DW13T
          M 85
          N 27
DW13F
          M 78
          N 29
DW14T
          M 79
          N 15
DW14F
          M 76
          N 17
DW15T
          M 77
          N  4
DW15F
          M 72
          N  7
DS00
          M 11
          N 93
DS01
          M 12
```

1293

	N 87
DS02	
	M 13
	N 73
DS03	
	M 14
	N 61
DS04	
	M 15
	N 53
DS05	
	M 20
	N 33
DS06	
	M 48
	N 19
DS07	
	M 49
	N 5
DS08	
	M 52
	N 91
DS09	
	M 53
	N 79
DS10	
	M 46
	N 67
DS11	
	M 47
	N 55
DS12	
	M 93
	N 41
DS13	
	M 90
	N 25
DS14	
	M 91
	N 13
DS15	
	M 88

BACKPLANE
PART-2

```
          N  3
B0CTC
          M 71
          G 49
          G 50
B0ITC
          M 30
          G 75
          G 76
B4OTC
          M 70
          G 15
          G 16
B4ITC
          M 37
          G 57
          G 58
BCITI
          M 36
BCOTI
          M 73
P13V
          G 42
          G 54
          J 42
          J 54
          L 42
          L 54
          N 42
          N 54
M07V
          G 46
          J 46
          L 46
          N 46
GND
          G 47
          G 47
          G 48
          G 49
          G 50
          G 51
```

J 47
J 48
J 49
J 50
J 51
L 47
L 48
L 49
L 50
L 51
N 47
N 48
N 49
N 50
N 51
Q 1
Q 2
Q 33
Q 34
Q 64
Q 63
Q 99
Q100
R 1
R 2
R 33
R 34
R 63
R 64
R 99
R100
S 1
S 2
S 33
S 34
S 63
S 64
S 99
S100
T 1
T 2
T 33

```
T 34
T 63
T 64
T 99
T100
M5R2V
G  3
G  4
G 35
G 36
G 65
G 66
G 97
G 98
R  3
R  4
R 35
R 36
R 65
R 66
R 97
R 98
S  3
S  4
S 35
S 36
S 65
S 66
S 97
S 98
T  3
T  4
T 35
T 36
T 65
T 66
T 97
T 98
M2V
Q  5
Q  6
Q 37
```

G 38
G 67
G 68
G 95
G 96
R 5
R 6
R 37
R 38
R 67
R 68
R 95
R 96
S 5
S 6
S 37
S 38
S 67
S 68
S 95
S 96
T 5
T 6
T 37
T 38
T 67
T 68
T 95
T 96

I10F1

G 7
G 8
R 75
R 76

P5V

G 31
G 32
G 62
G 61

B13F

G 45
G 46

```
B13T
          Q 47
          Q 48
R8F
          Q 51
          Q 52
          S 41
          S 42
R8T
          Q 53
          Q 54
          S 43
          S 44
OVFL
          Q 83
          Q 84
          R 49
          R 50
          S 55
          S 56
          T 49
          T 50
B12F3
          Q 87
          Q 88
          T 89
          T 90
B12F2
          Q 89
          Q 90
          S 47
          S 48
B12T3
          Q 91
          Q 92
B12T2
          Q 93
          Q 94
          S 45
          S 46
C3F
          R  9
```

182

```
          R 10
          S 85
          S 86
C2T2
          R 11
          R 12
          S 89
          S 90
I10F2
          R 77
          R 78
          T 87
          T 88
S42T
          R 79
          R 80
          T 85
          T 86
I3T
          R 87
          R 88
          S 93
          S 94
I4F
          R 89
          R 90
          S 87
          S 88
S23F
          S  9
          S 10
          T  7
          T  8
S22F
          S 51
          S 52
          T  9
          T 10
CCNLEN
          T 79
          T 80
IN1
```

```
            C 62
ICBFC
            C 63
            C  4
            D 63
            D  4
            E 72
ICOFA
            C  8
            C 80
            D  8
            D 80
            E 65
MCK1
            C 96
            C 24
            D 96
            D 24
            E 73
MCK2
            C 94
            C 25
            D 94
            D 25
            E 88
OSRLF
            C 85
            C 15
            D 85
            D 15
            E 20
OUT1
            C 83
MUXA2
            C 58
            D 58
            E 85
MUXB2
            C 61
            D 61
            E 94
MUXC2
```

1847

```
          C 60
          D 60
          E 71
OBFC
          C 86
          C 16
          D 86
          D 16
          E 38
INO
          C  3
GIDF
          C 40
          D 40
          E 21
GBDF
          C 41
          D 41
          E 67
GFDF
          C 38
          D 38
          E 89
MUXA1
          C  7
          D  7
          E 84
MUXB1
          C  6
          D  6
          E 96
MUXC1
          C  5
          D  5
          E 70
OUTO
          C 12
VDD1                          MINUS
          C  9
          D  9
VDD2                          VOLT
          C 10
```

D 10

VDD3

C 36
D 36

VDD4

C 39
D 39

VDD5

C 64
D 64

VDD6

C 65
D 65

VDD7

C 92
D 92

VDD8

C 95
D 95

IN3

D 62

OUT3

D 83

IN2

D 3

OUT2

D 12

ICBT

E 54

ICAT

E 55

LCW

E 74

MED

E 75

HI

E 68

512

E 69

1K

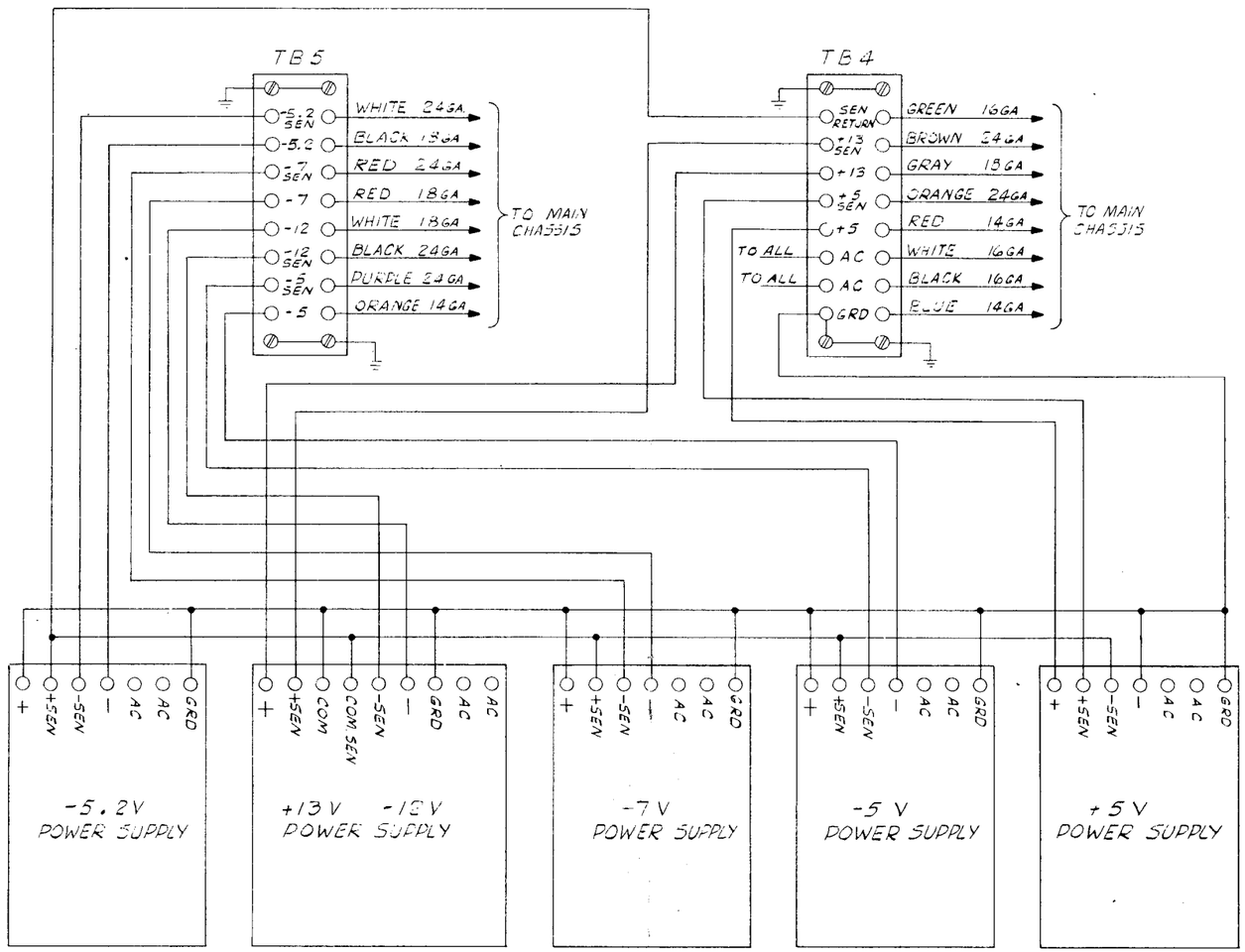
E 76

2K

WIRED

```
        E 77
4K
        E 66
8K
        E 95
16K
        E 92
32K
        E 93
64K
        E 90
NSUP
        E  7
NSDN
        E  6
MCF
        E 39
NDSYC
        E 78
```

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED

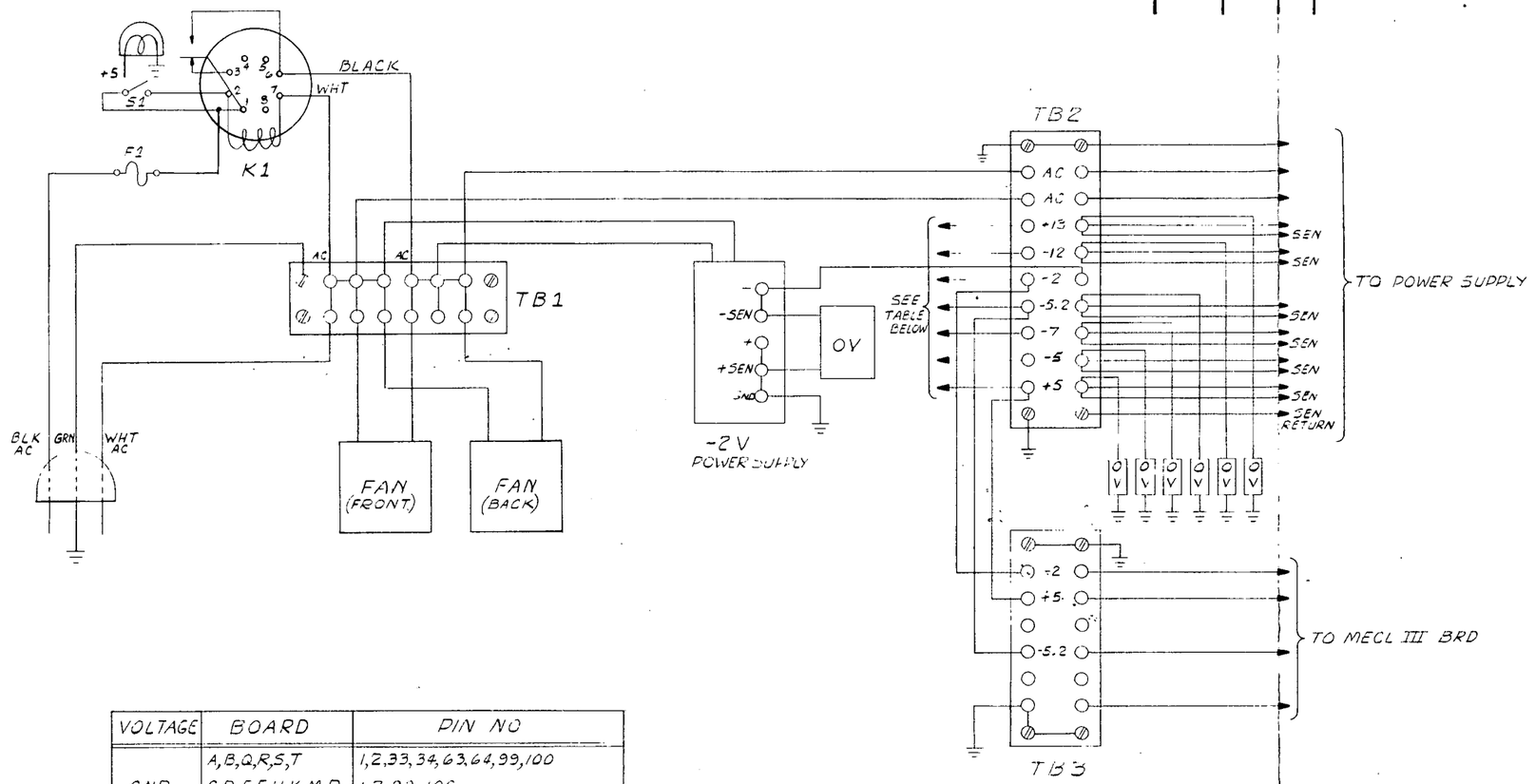


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS 6-N1	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY S. CRAYTON DATE 1975	TITLE: POWER SUPPLY UNIT WIRING DIAGRAM
SURFACES ✓	CHECK	
MATERIAL	ENGINEER	
SPEC	PROJECT	SIZE C · CODE IDENT NO. 11617 · DWG NO. WE 1025
		SCALE — · WEIGHT — · SHEET 1 OF 1

FOLDOUT FRAME

FOLDOUT FRAME

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



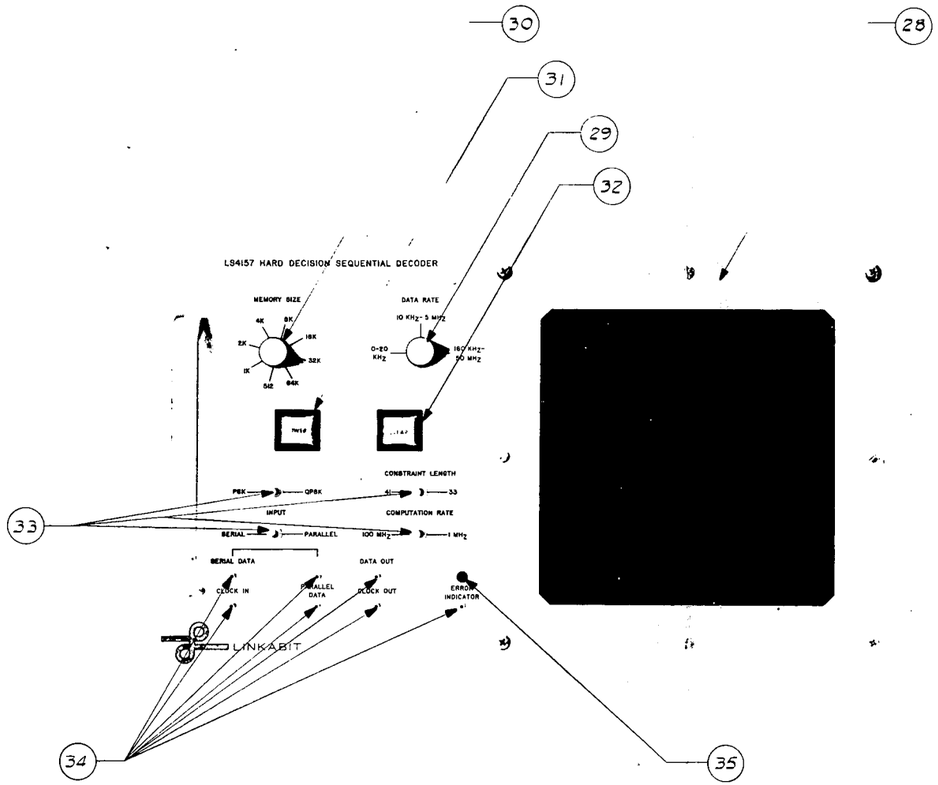
VOLTAGE	BOARD	PIN NO
GND	A,B,Q,R,S,T	1,2,33,34,63,64,99,100
	C,D,E,F,H,K,M,P	1,2,99,100
	G,J,L,N	1,2,8,47,48,49,50,82,99,100
+5.0	A	15
	C,D,E,F,H,K,M,P	97, 98
	G,J,L,N	24
	Q	31,32
-5.2	A,B,Q,R,S,T	3,4,35,36,65,66,97,98
-2.0	A B Q R S T	5,6,37,38,67,68,95,96
+13.0	G J L N	42,54
-7.0	G J L N	46
-12.0	C D	11,13,36,39,64,65,89,95
-5.0	C D	9,10,20,44,56,79,92,93

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS 5-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY S. GRAYTON DATE 7/72	TITLE MAIN CHASSIS POWER WIRING
MATERIAL	CHECK	
SPEC	ENGINEER	
	PROJECT	
	SIZE C	CODE IDENT NO. 11617
	DWG NO. WD 102 D	
	SCALE –	WEIGHT –
	SHEET 1 OF 1	

FOLDOUT FRAME 1

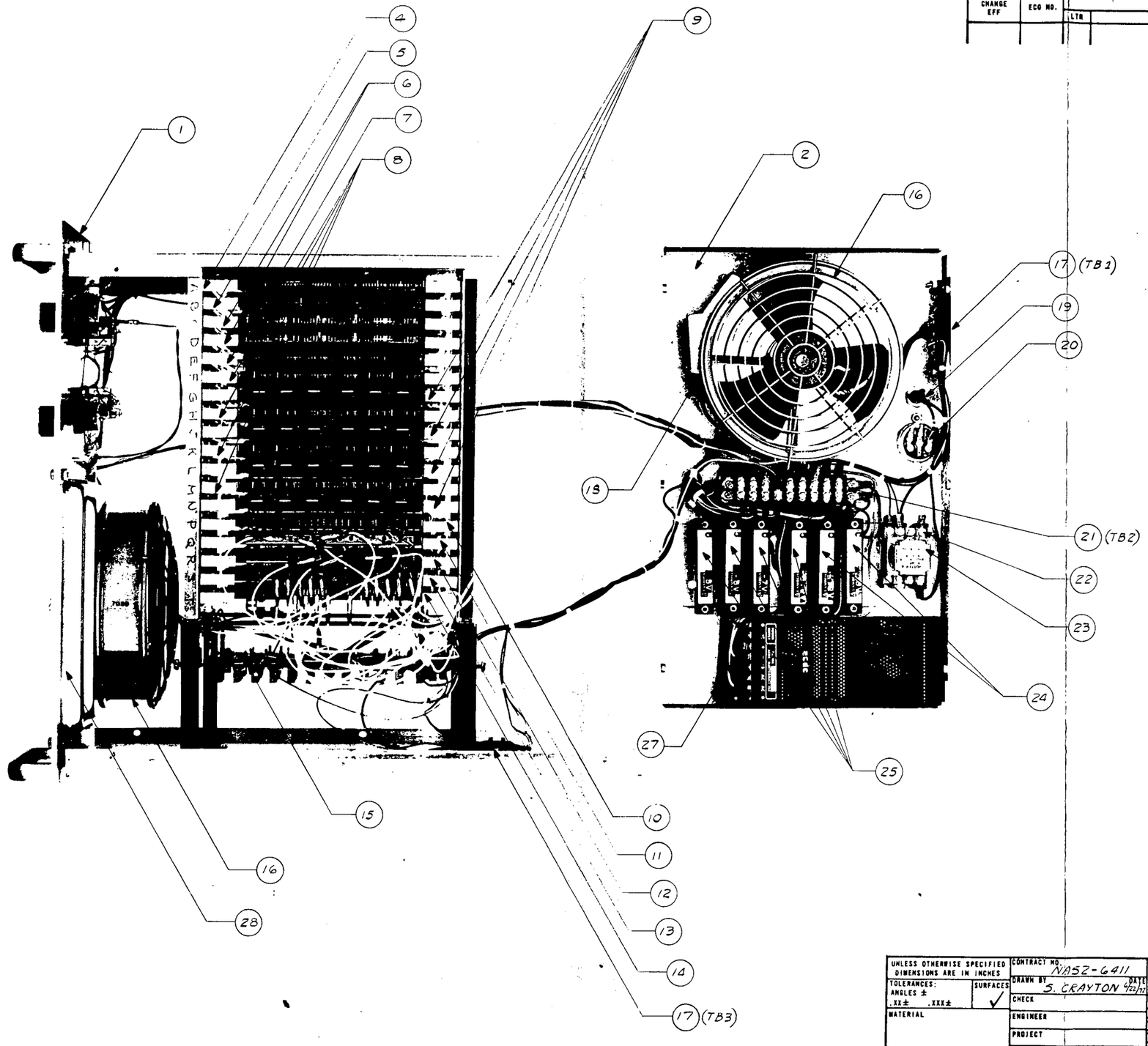
FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY S. CRAYTON DATE 7/31/79	TITLE HDSD TOP ASSY
MATERIAL		CHECK	
SPEC		ENGINEER	
		PROJECT	SIZE C / CODE IDENT NO. 11627 / DWG NO. 1000342
			SCALE - / WEIGHT - / SHEET 1 OF 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED

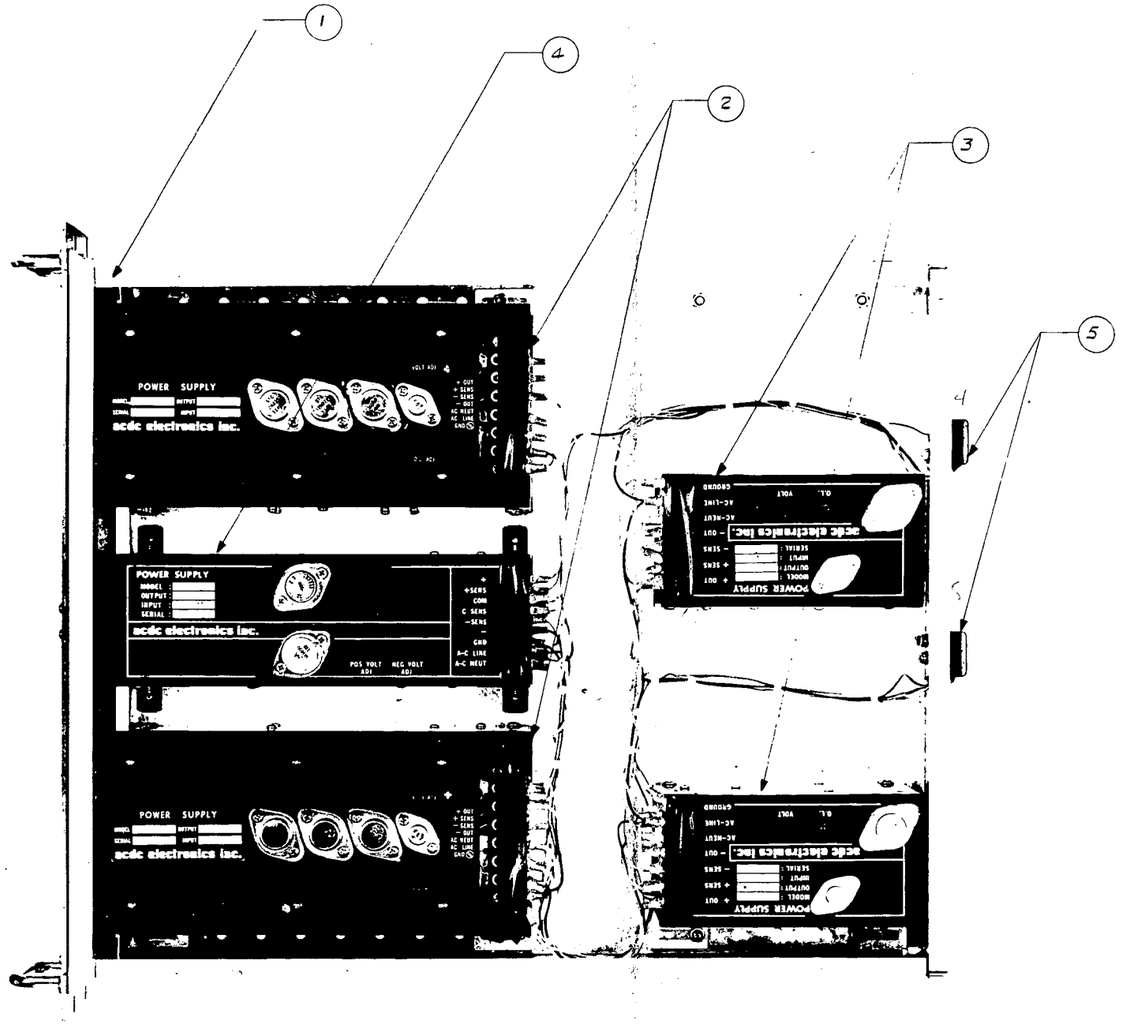


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY S. CRAYTON DATE 4/22/77	TITLE HDSD TOP ASSY
MATERIAL	CHECK	
	ENGINEER	
SPEC	PROJECT	SIZE C · CODE IDENT NO. 11627 · DWG NO. 1000342
		SCALE - · WEIGHT - · SHEET 2 OF 2

FOLDOUT FRAME 1

FOLDOUT FRAME 2

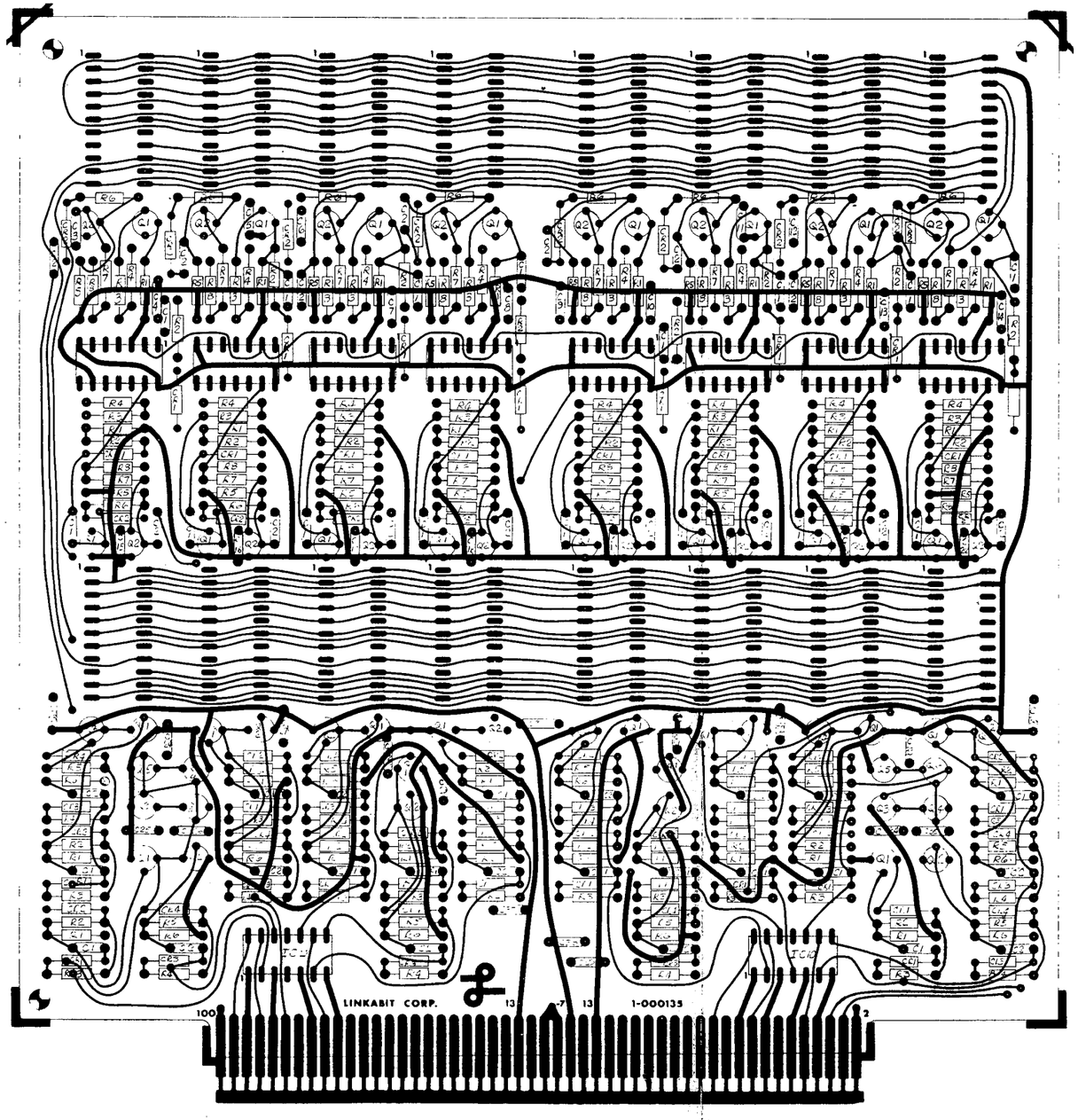
CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX ± .XXX ± / SURFACES ✓	DRAWN BY S. CRAYTON DATE 9/21/71	TITLE HDSD POWER SUPPLY UNIT
MATERIAL	CHECK	SIZE C / CODE IDENT NO. 11627 / DWG NO. 1000343
SPEC	ENGINEER	SCALE – / WEIGHT – / SHEET 1 OF 1
	PROJECT	

FOLDOUT FRAME 1

FOLDOUT FRAME 2



COMP SIDE 1

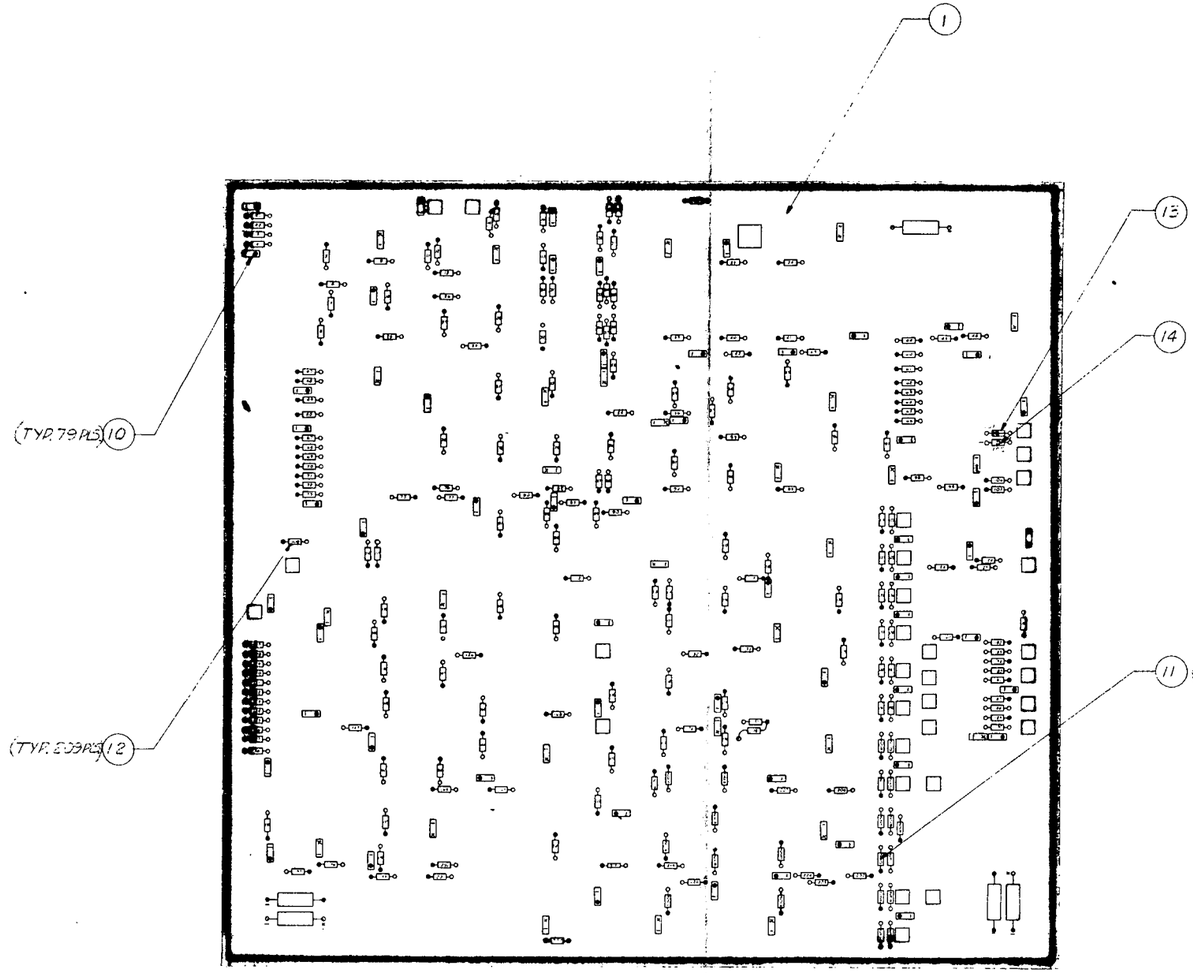
NOTE
FOR LIST OF PARTS
SEE LMI-000149

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO.	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY / DATE	TITLE PCB ASSY MAIN MEMORY BOARD
SURFACES ✓	CHECK	
MATERIAL	ENGINEER	
SPEC	PROJECT	SIZE D · CODE IDENT NO. 11657 · DWG NO. 1000149
		SCALE 2X · WEIGHT – · SHEET 1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED



COMPONENT MOUNTING
SIDE - 1

NOTES

1. LOCATIONS FOR I.C'S SHOWN ON BOARD.

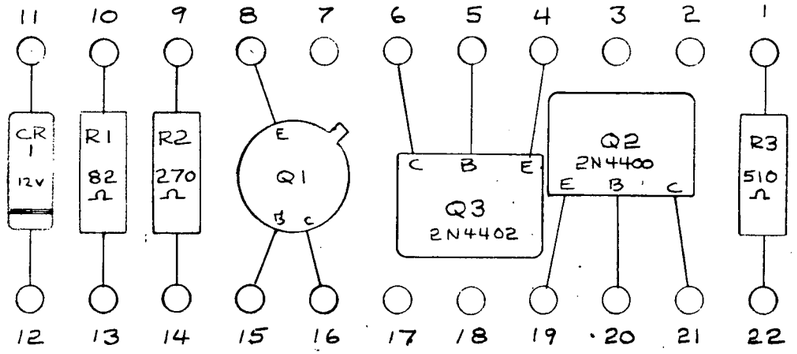
FOR LIST OF PARTS SEE PL1000186

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS5-3411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± / SURFACES ✓	DRAWN BY S. CRAYTON DATE 7/4/69	TITLE: HDSD ALGORITHM LOGIC P.C. BOARD ASSEMBLY
MATERIAL	CHECK	
	ENGINEER	
SPEC	PROJECT	SIZE C · CODE IDENT NO. 11697 · DWG NO. 1000186
		SCALE · WEIGHT · SHEET 1 OF 1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



Vcc +5 VOLTS DXX-1, DXX-21

VDD -10 VOLTS DXX-6, DXX-8, DXX-9

INPUT DXX-12

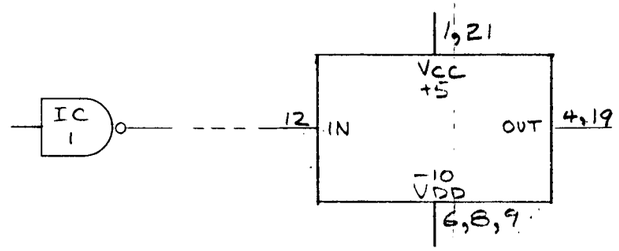
OUTPUT DXX-4, DXX-19

INTERNAL CONNECTIONS

DXX-10 TO DXX-11

DXX-13 TO DXX-14 TO DXX-15

DXX-16 TO DXX-5 TO DXX-20 TO DXX-22

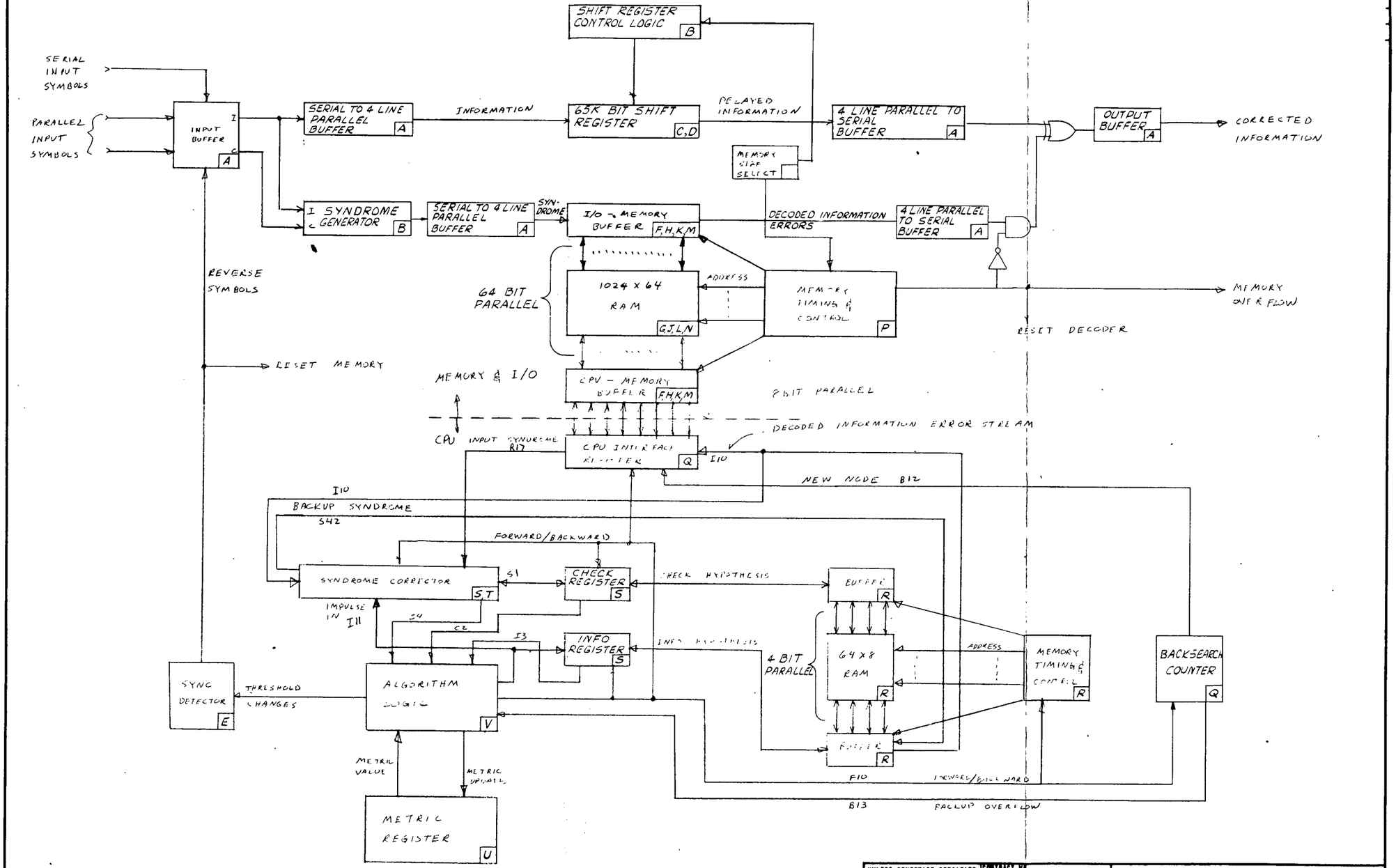


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. 6000	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± / SURFACES ✓	DRAWN BY JC DATE 8/1/1	TITLE INFO MEMORY CLOCK DRIVER
MATERIAL	CHECK	
SPEC	ENGINEER	SIZE / CODE IDENT NO. 11627 / DWG NO. 1000333
	PROJECT	SCALE / WEIGHT / SHEET 1 OF 1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED

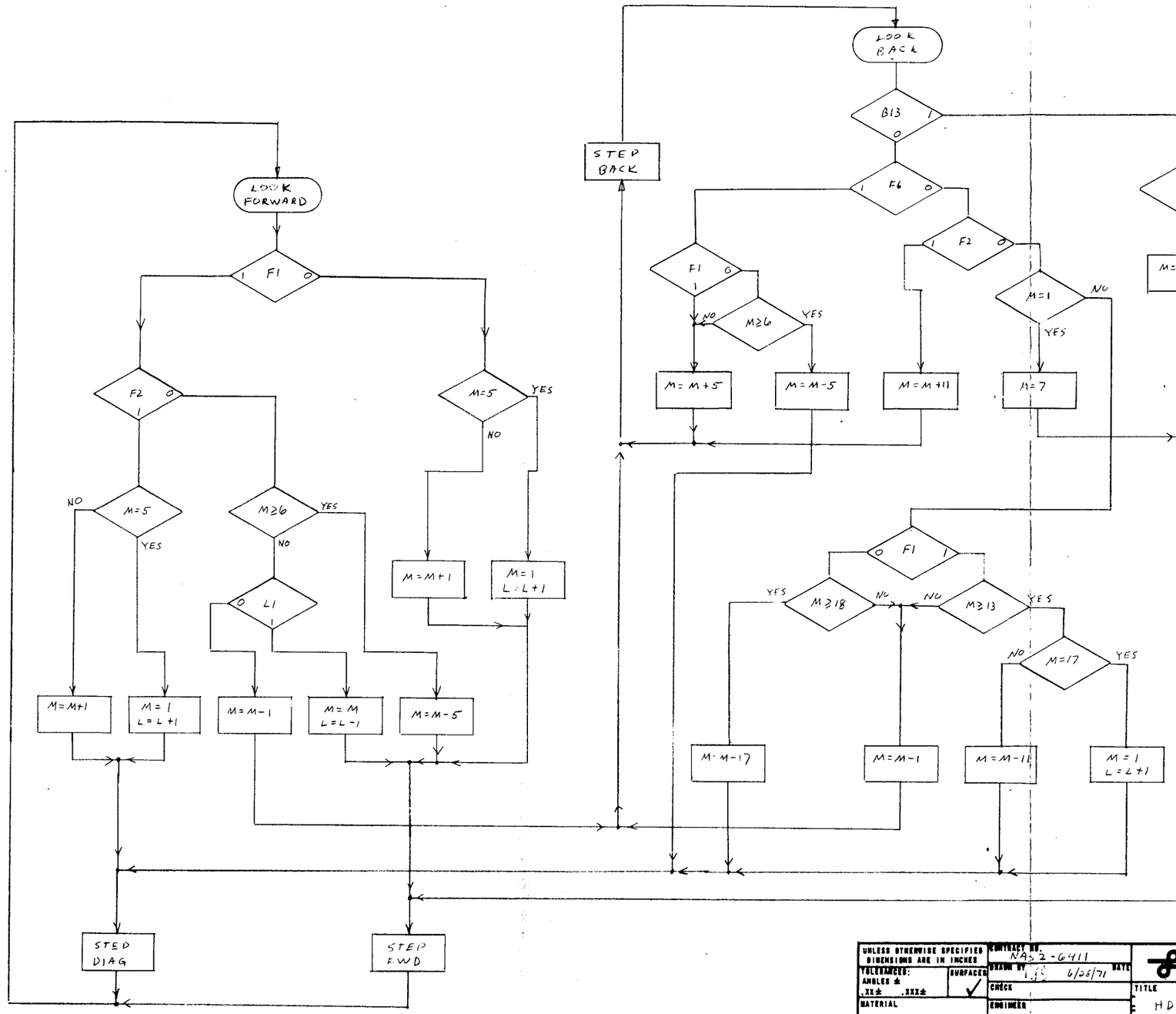


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY KDS 4/22/71 DATE	TITLE HDSD BLOCK DIAGRAM
MATERIAL	CHECK	
SPEC	ENGINEER	
	PROJECT	SIZE C · CODE IDENT NO. 11515 · DWG NO. 2-000155 · SCALE — · WEIGHT — · SHEET 1 OF 2

FOLDOUT FRAME 1

FOLDOUT FRAME 1

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED

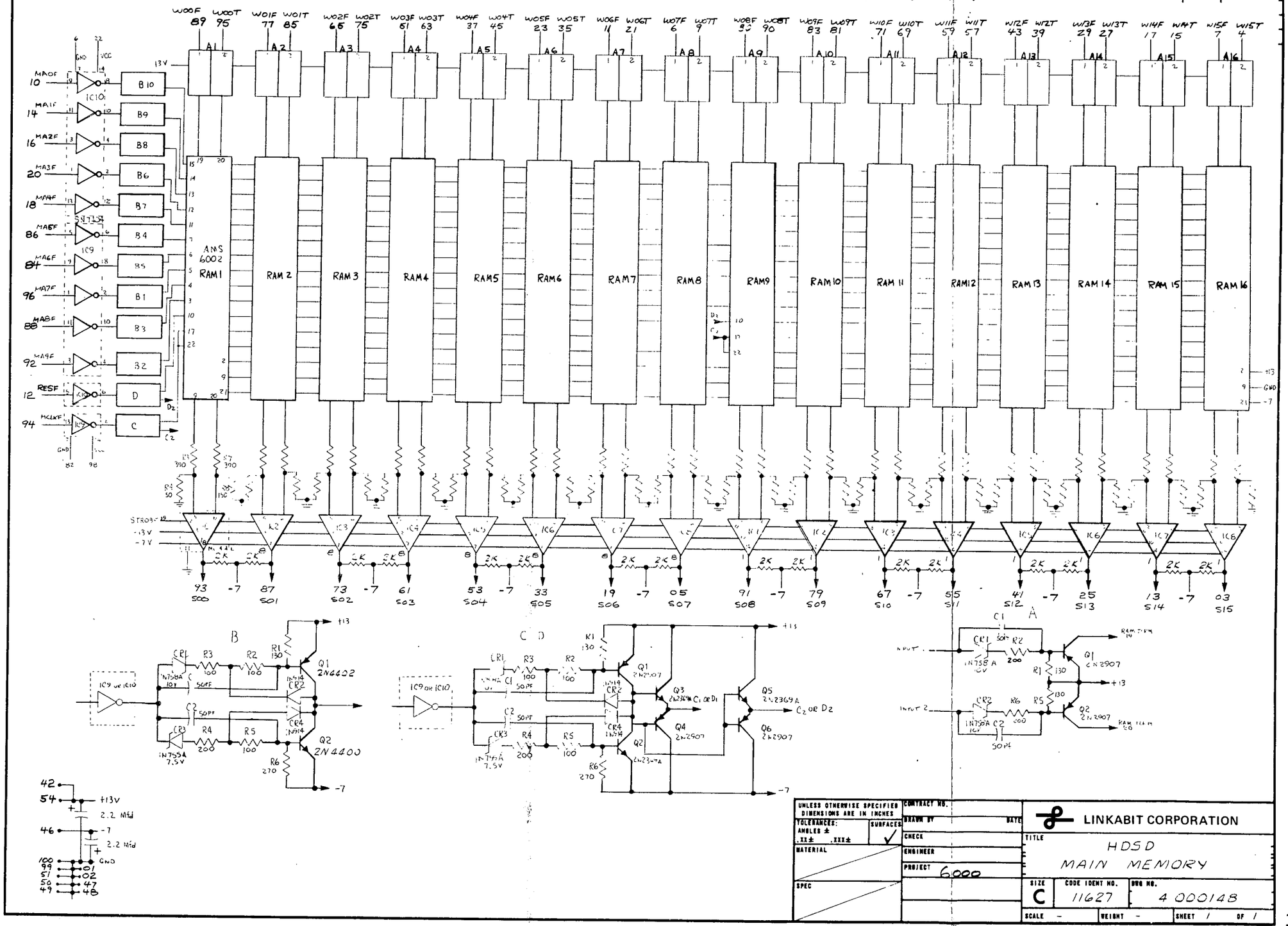


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY 6/28/71 DATE	TITLE HDSD ALGORITHM
MATERIAL	CHECK	
SPEC	ENGINEER	
	PROJECT	
	SIZE C	CODE IDENT NO. 11627
	DWG NO. 2-000155	
	SCALE	WEIGHT
	SHEET 2 OF 2	

FOLDOUT FRAME 1

FOLDOUT FRAME 2 197<

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± .XX± .XXX±
SURFACES
MATERIAL
SPEC

CONTRACT NO.
DRAWN BY DATE
CHECK
ENGINEER
PROJECT 6000

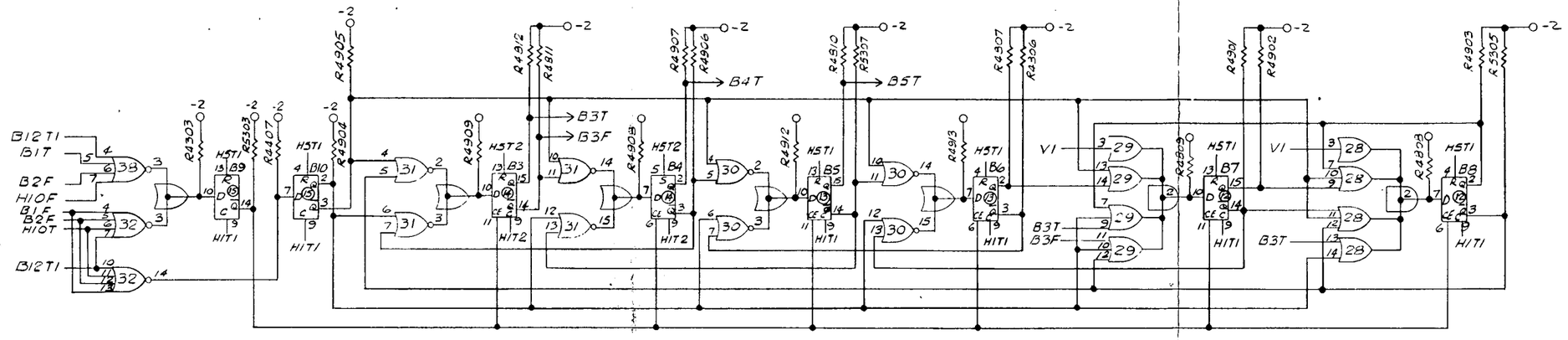
LINKABIT CORPORATION

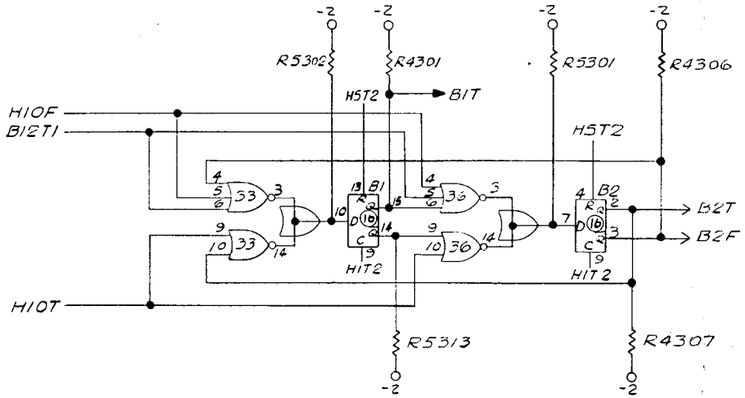
TITLE
HDSD
MAIN MEMORY

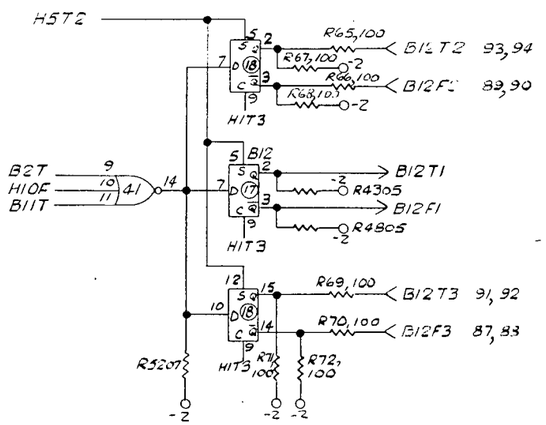
SIZE C | CODE IDENT NO. 11627 | DWG NO. 4 000148

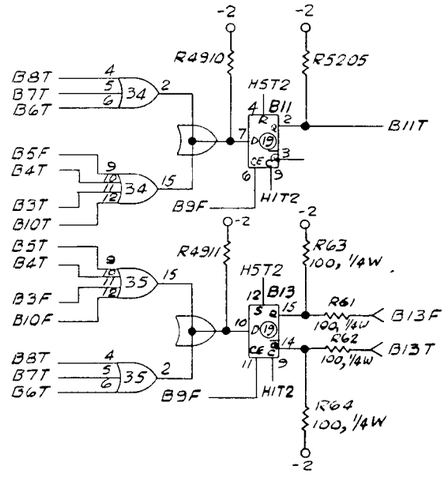
SCALE - | WEIGHT - | SHEET 1 OF 1

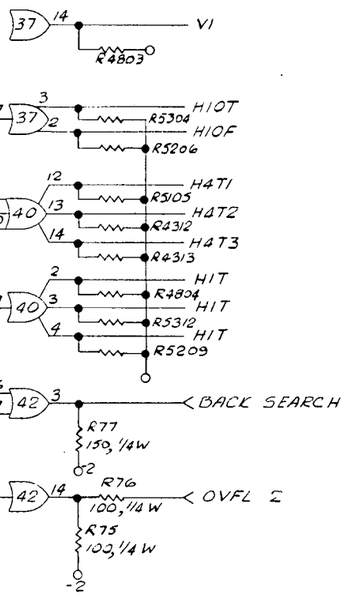
CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED





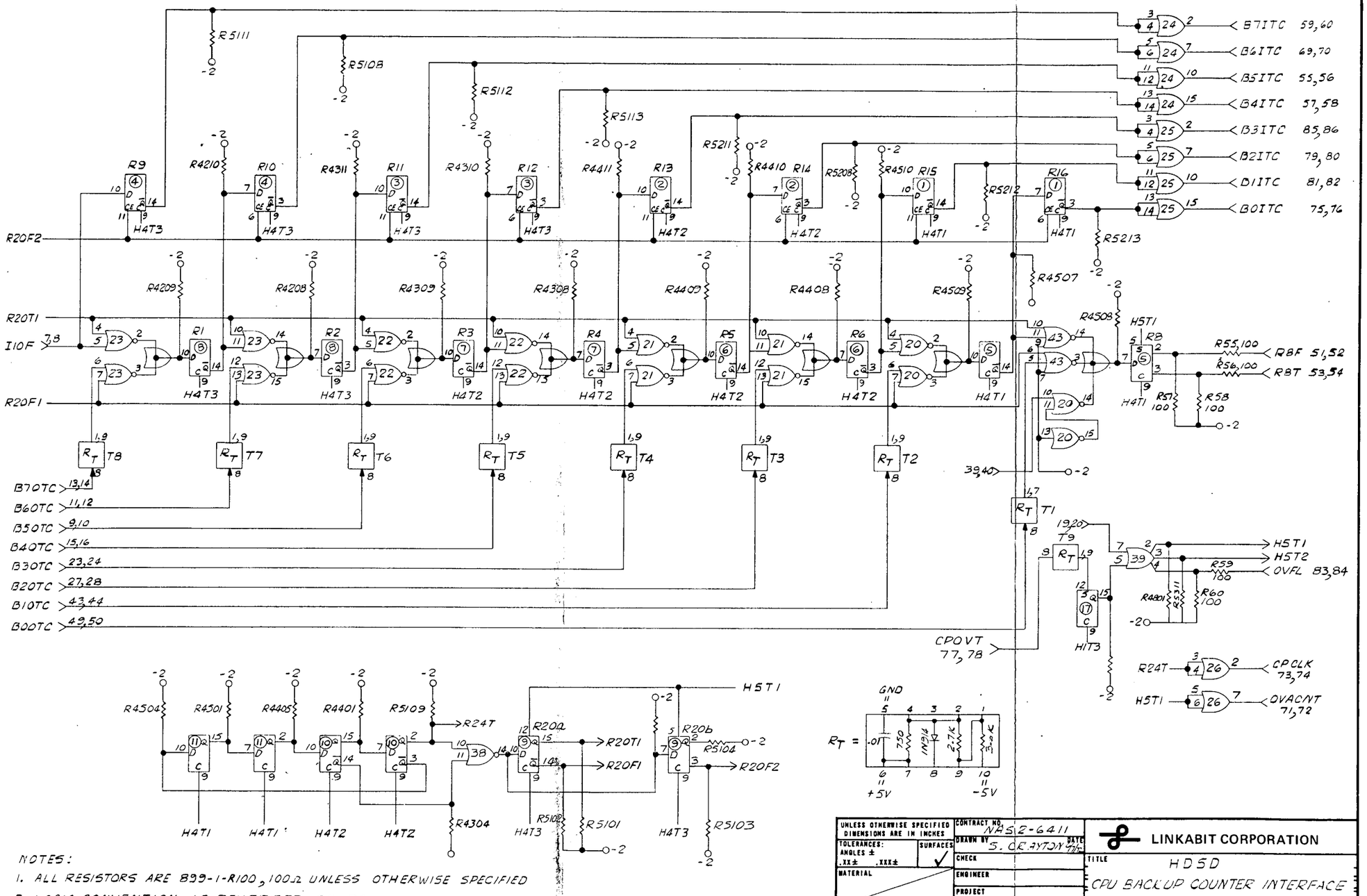






UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NA52-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY S. CRAYTON	DATE 9/1/78	TITLE HDSD CPU BACKUP COUNTER INTERFACE
SURFACES ✓	CHECK		
MATERIAL	ENGINEER		
SPEC	PROJECT		SIZE C · CODE IDENT NO. 11627 · DWG NO. 4-000151
			SCALE · WEIGHT · SHEET 1 OF 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



NOTES:

1. ALL RESISTORS ARE 899-1-R100, 100Ω UNLESS OTHERWISE SPECIFIED
2. LOGIC CONVENTION IS REVERSED ON R8

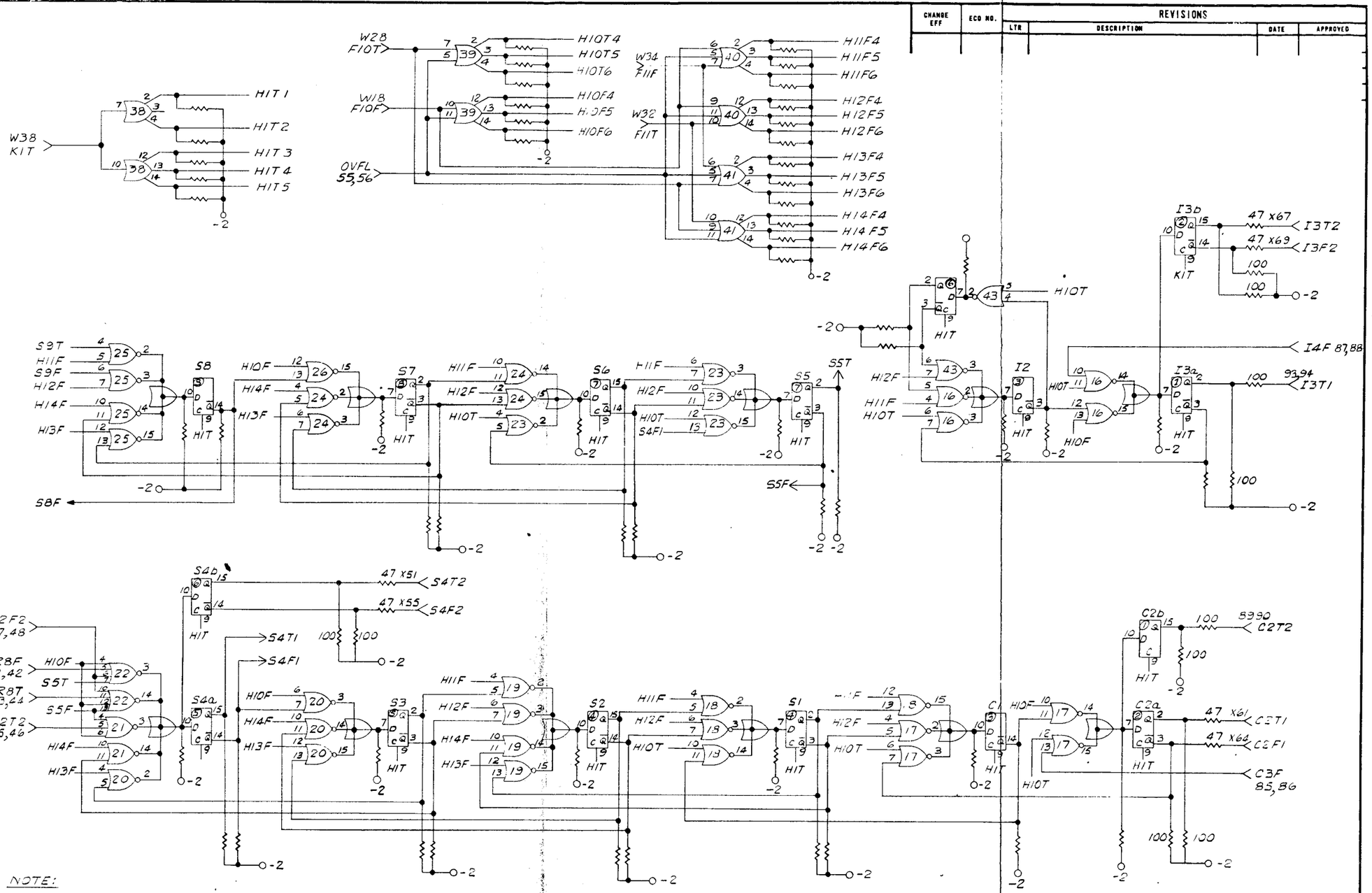
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS12-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY S. OKAYDIN DATE 7/7/	TITLE HDSD CPU BACKUP COUNTER INTERFACE
SURFACES ✓	CHECK	
MATERIAL	ENGINEER	SIZE C · CODE IDENT NO. 11627 · DWG NO. 4-000151
SPEC	PROJECT	SCALE – · WEIGHT – · SHEET 2 OF 2

FOLDOUT FRAME 1

FOLDOUT FRAME 2

200

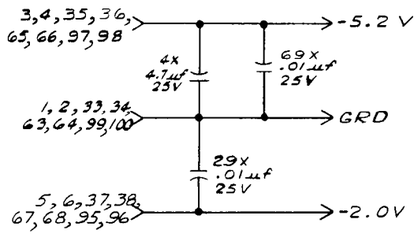
CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED

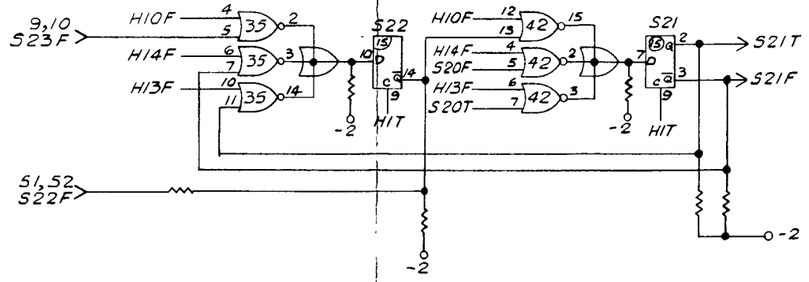


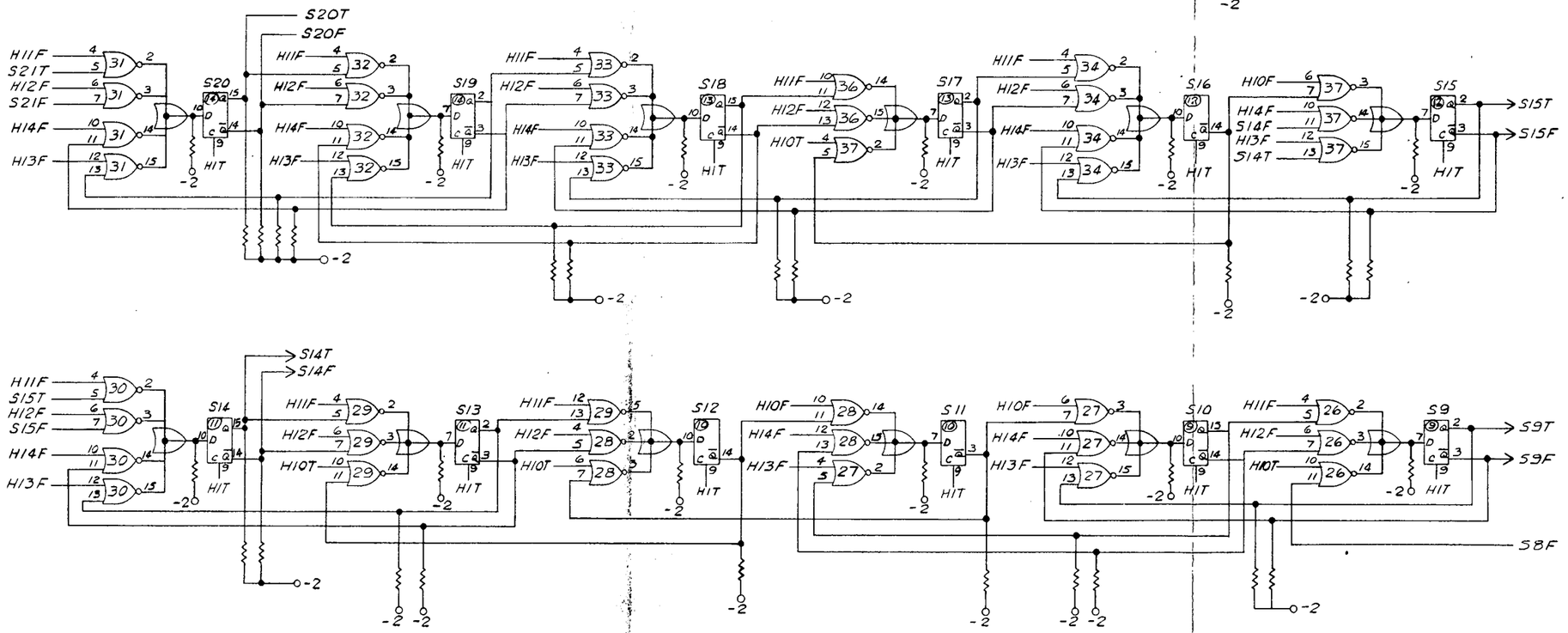
NOTE:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 899-1-R100

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NASA-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY S. CLAYTON 3-[illegible]	TITLE HD5D CPU SYNDROME CORRECTOR #1 BITS 1-8
SURFACES ✓	CHECK	
MATERIAL —	ENGINEER	SIZE C · CODE IDENT NO. 11617 · DWG NO. 4-000152
SPEC —	PROJECT	SCALE — · WEIGHT — · SHEET 1 OF 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED

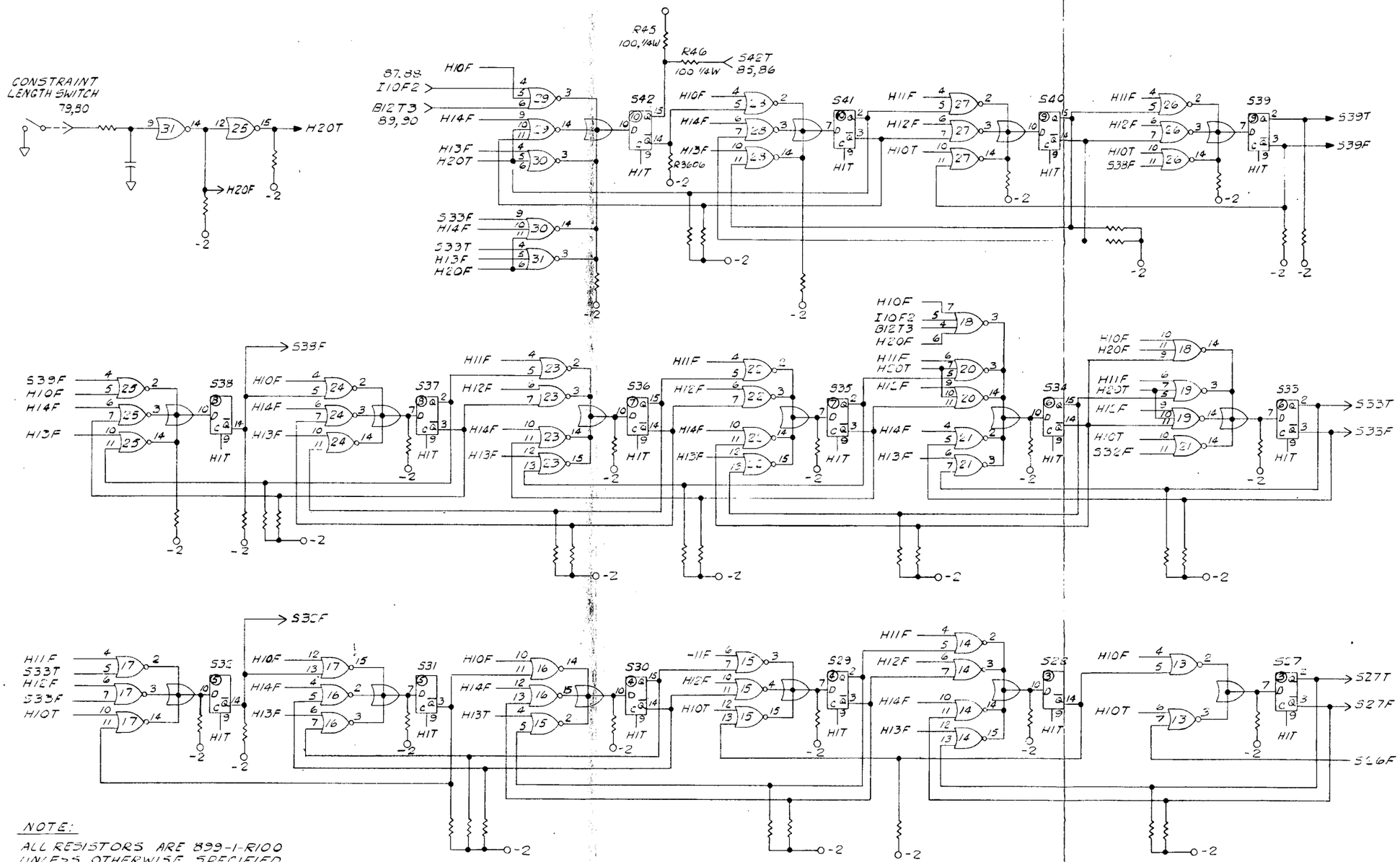






UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NA52-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY S. CRAYTON DATE 2/1/	TITLE HDSD CPU SYNDROME CORRECTOR #1 BITS 9-26
MATERIAL —	CHECK	SIZE C CODE IDENT NO. DWG NO. 4-000152
SPEC —	ENGINEER	SCALE — WEIGHT — SHEET 2 OF 2
	PROJECT	

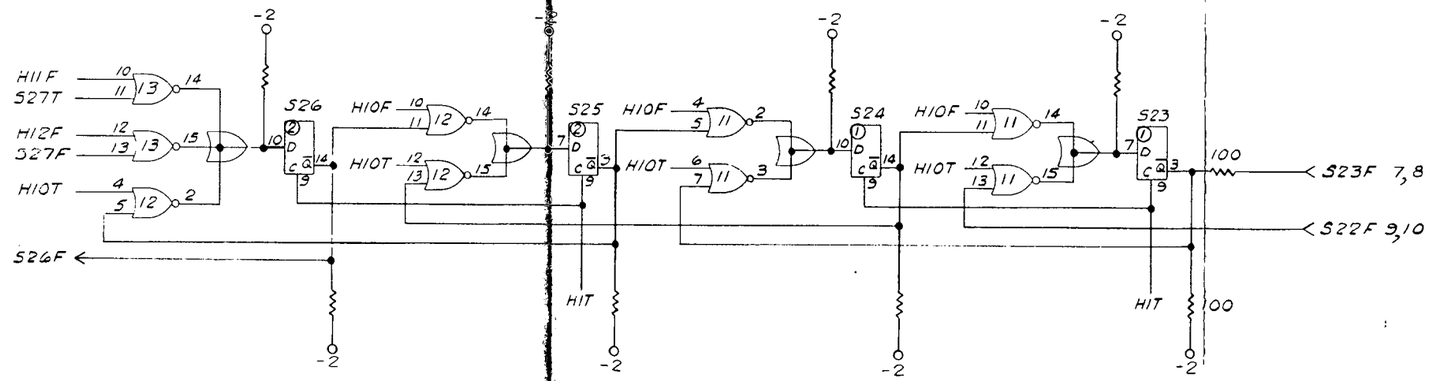
CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED

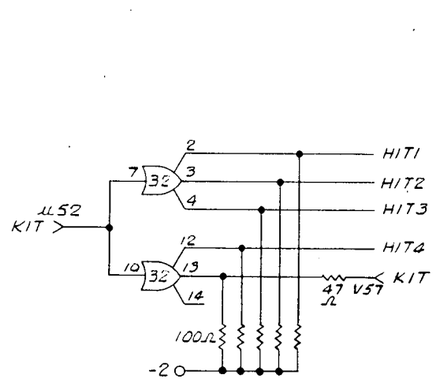


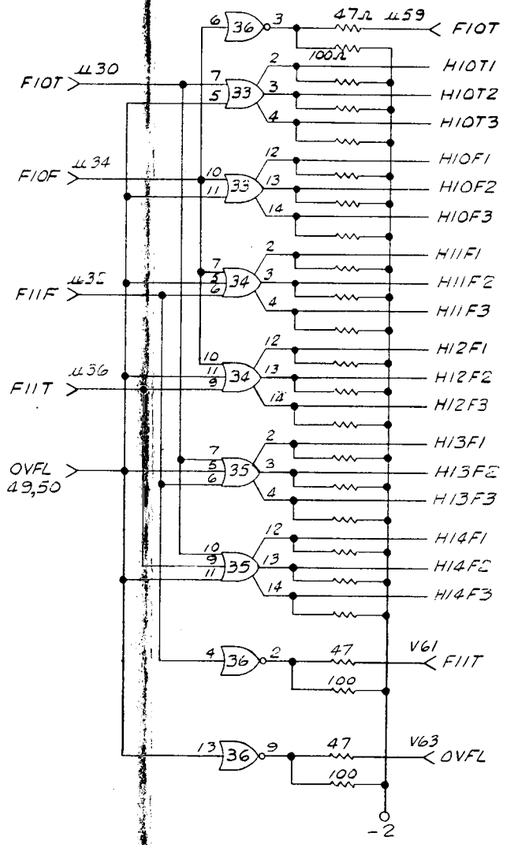
NOTE:
ALL RESISTORS ARE 899-1-R100
UNLESS OTHERWISE SPECIFIED

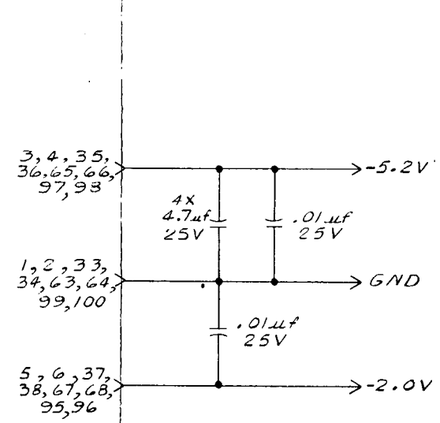
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS1-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY S. CRAYTON DATE 12/71	TITLE HDSD CDU SYNDROME CORRECTOR #2 BITS 27-42
MATERIAL	CHECK	
SPEC	ENGINEER	
	PROJECT	SIZE C · CODE IDENT NO. 11607 · DRG NO. 4-000153
		SCALE — · WEIGHT — · SHEET 1 OF 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED







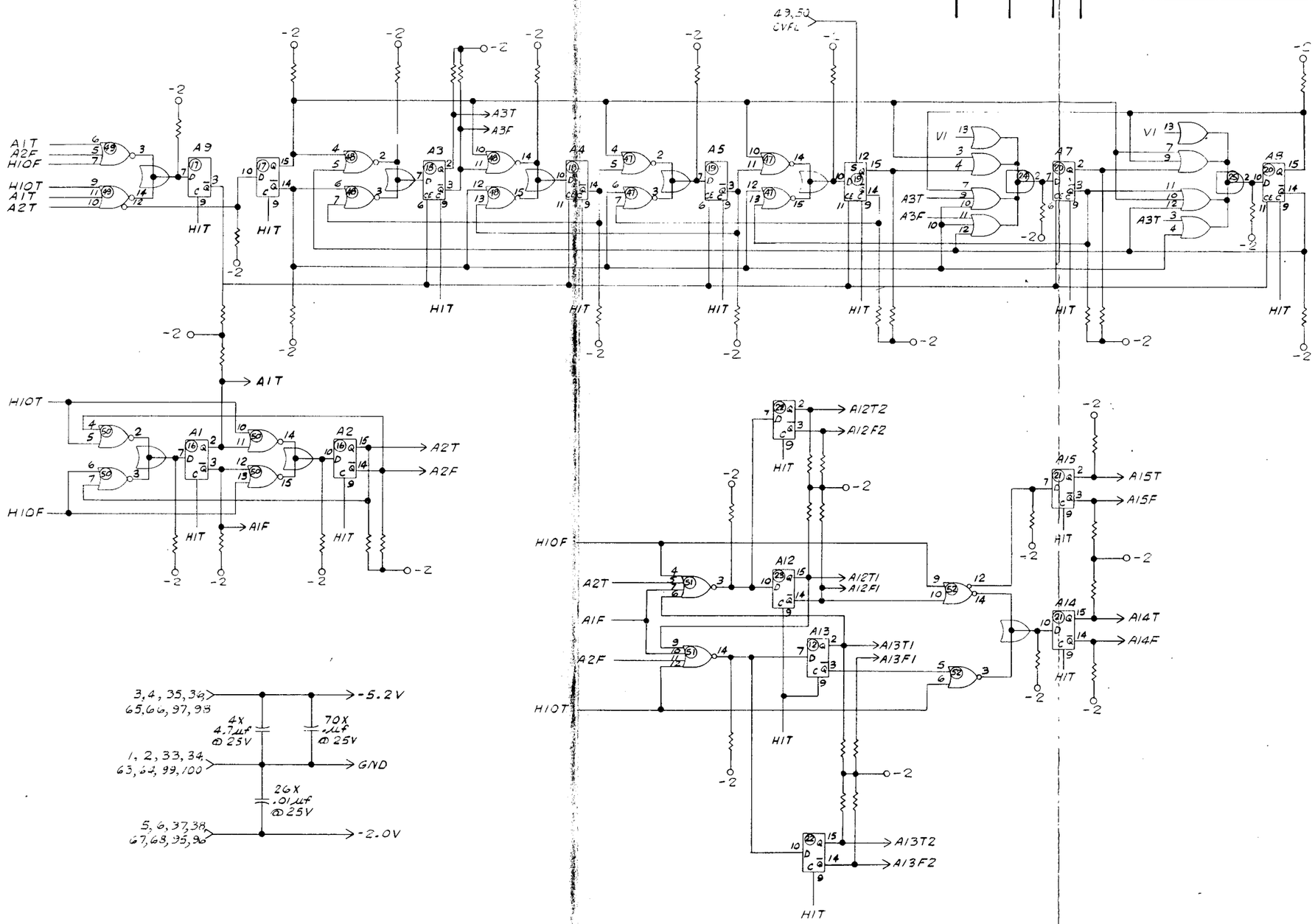


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY S. CRAYTON DATE 4/25/73	TITLE	CPU SYNDROME CORRECTOR #2
MATERIAL	CHECK		
SPEC	ENGINEER		
	PROJECT	SIZE C	CODE IDENT NO. 11627
		DWG NO.	4-000153
		SCALE	WEIGHT
		SHEET 2 OF 2	

FOLDOUT FRAME 1

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED

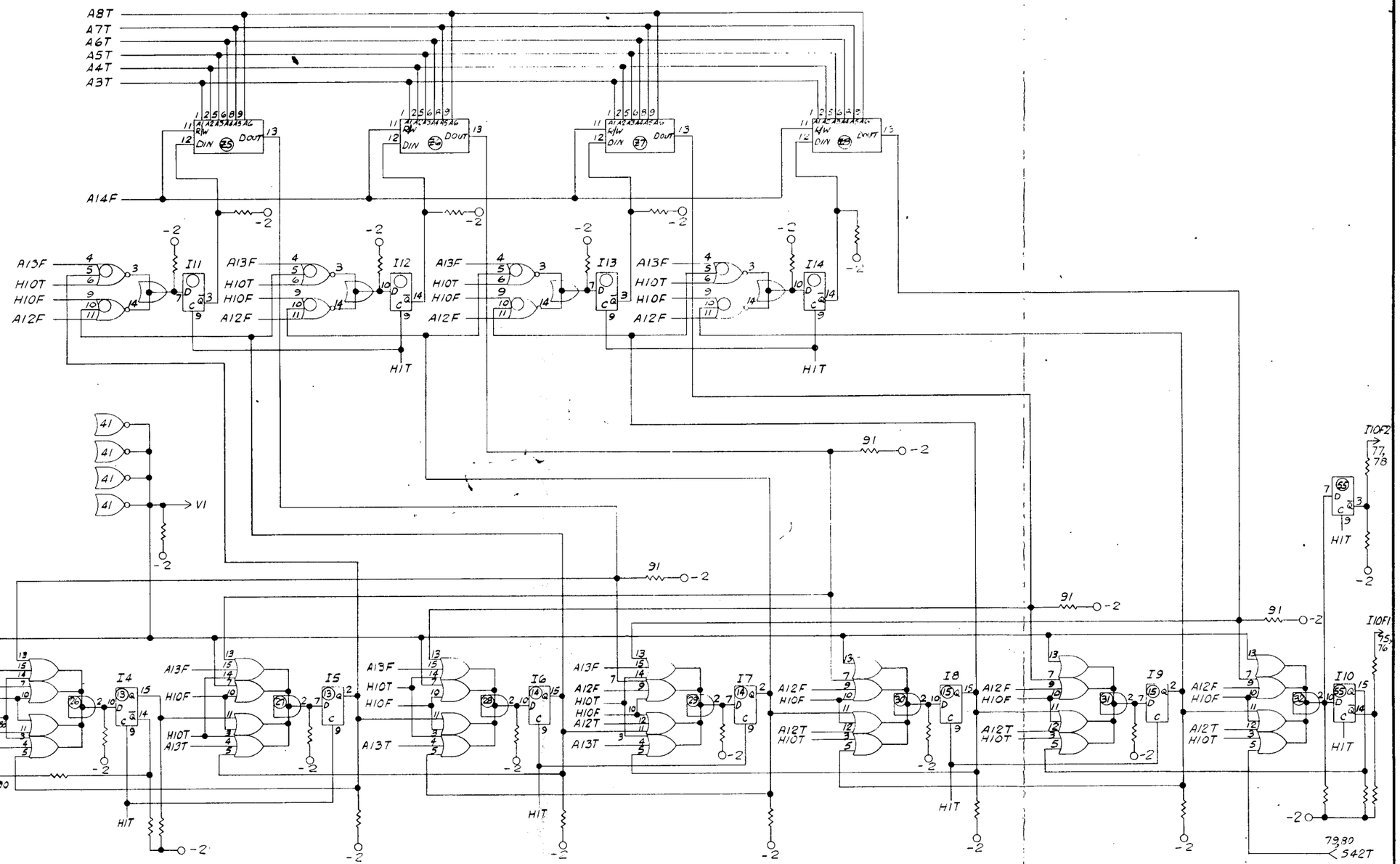


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY S. CRAYTON 5/24/72	TITLE HDSD CPU BACKUP BUFFER ADDRESS COUNTER AND CONTROL LOGIC
MATERIAL	CHECK	ENGINEER	SIZE C / CODE IDENT NO. 11627 / DWG NO. 4-000154
SPEC	PROJECT		SCALE – / WEIGHT – / SHEET 1 OF 3

FOLDOUT FRAME 1

205< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



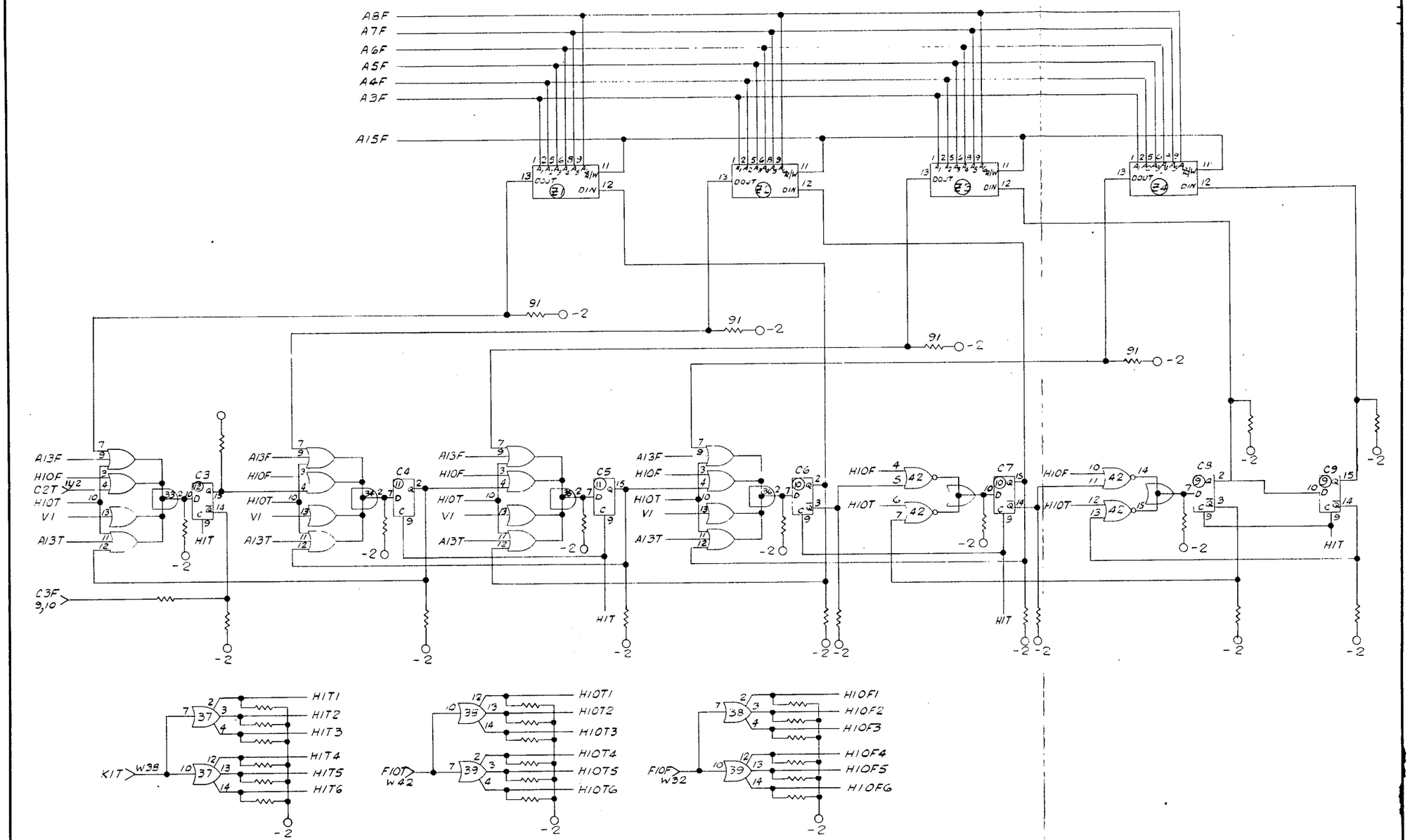
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY S. CRAYTON 4/17/72	TITLE HDSD CPU BACKUP BUFFER INFORMATION HYPOTHESIS
MATERIAL		CHECK	
SPEC		ENGINEER	
		PROJECT	SIZE C · CODE IDENT NO. 11627 · DWG NO. 4-000154
			SCALE — · WEIGHT — · SHEET 2 OF 3

FOLDOUT FRAME (

206<

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED



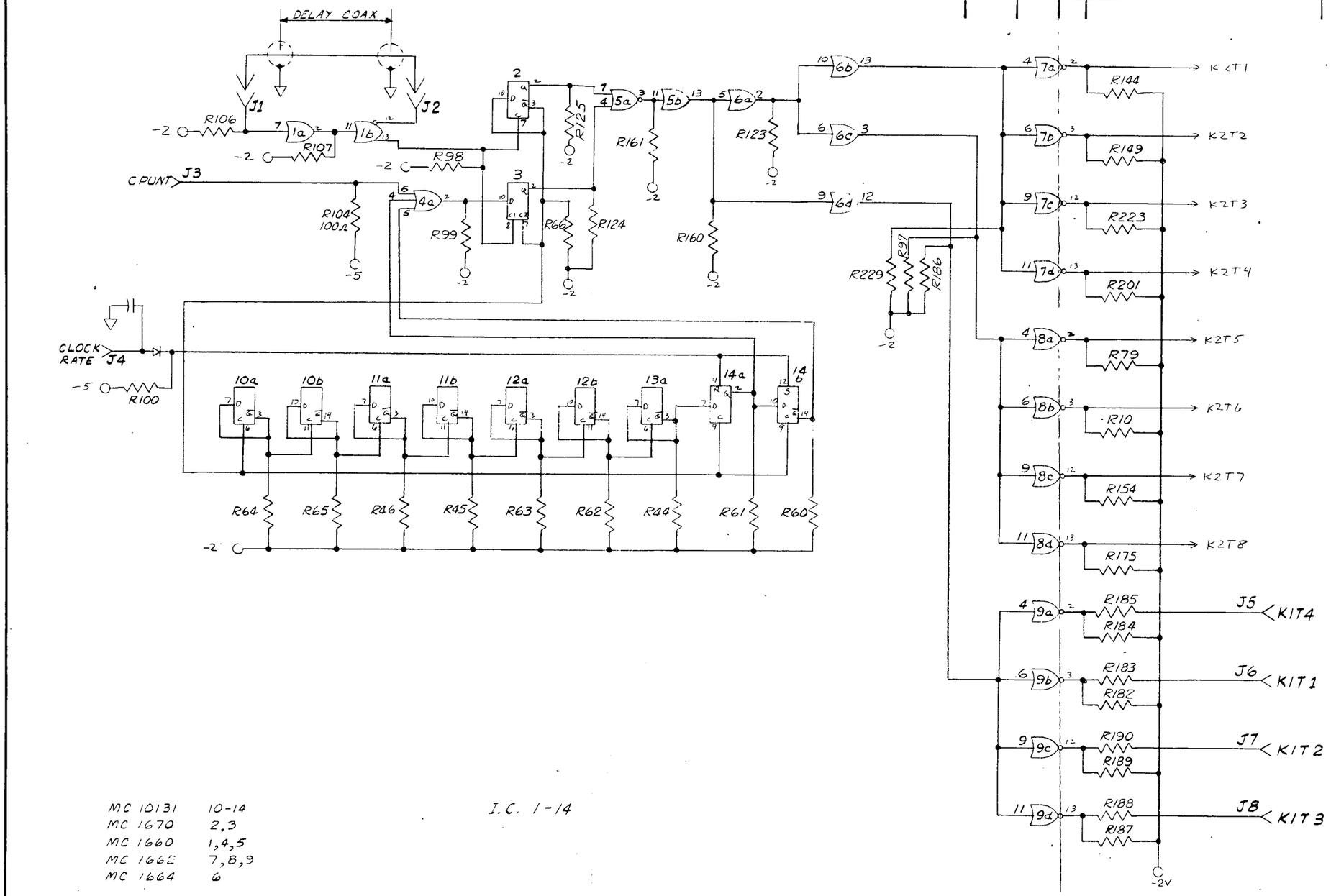
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY S. CRAYTON	DATE 5/18/	TITLE HDSD CPU BACKUP BUFFER CHECK HYPOTHESIS
SURFACES ✓	CHECK		
MATERIAL	ENGINEER		
SPEC	PROJECT		SIZE C · CODE IDENT NO. 11687 · DWG NO. 4-000154
			SCALE – · WEIGHT – · SHEET 3 OF 3

FOLDOUT FRAME 1

207

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



MC 10131	10-14
MC 1670	2,3
MC 1660	1,4,5
MC 1662	7,8,9
MC 1664	6

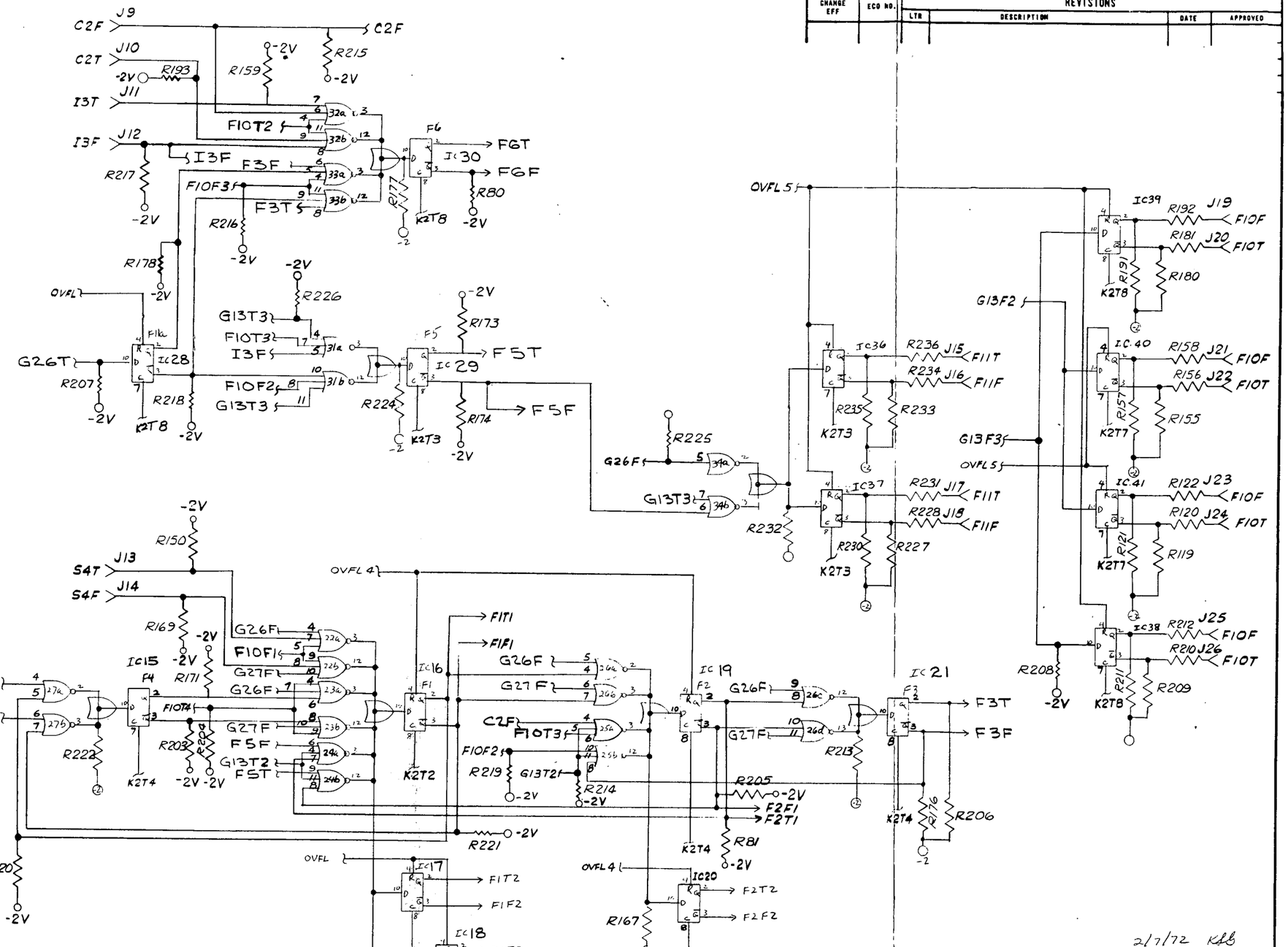
I.C. 1-14

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY [illegible] 5/1/71 DATE	TITLE	HDSD ALGORITHM LOGIC
MATERIAL	CHECK	SIZE C	CODE IDENT NO. 11627
SPEC	ENGINEER	DWG NO.	4-000156
	PROJECT	SCALE —	WEIGHT — SHEET 1 OF 6

FOLDOUT FRAME 1

208 FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



MC 1660 12-25, 31-33
MC 1662 26, 27, 34
MC 1670 15-21, 28-30, 36-41

I.C. 15-41
I.C. 35 NOT USED

2/7/72 KLB

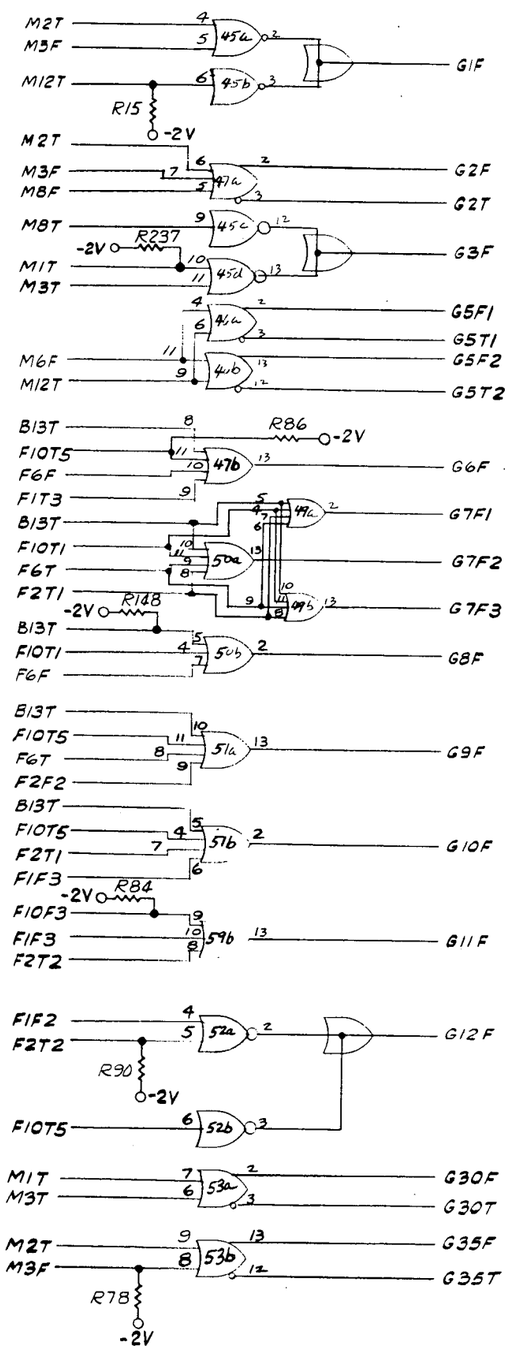
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6111	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY DATE	TITLE	HD5D ALGORITHM LOGIC
MATERIAL	CHECK		
	ENGINEER		
SPEC	PROJECT	SIZE C	CODE IDENT NO. 11627 DWG NO. .4-000156
		SCALE —	WEIGHT — SHEET 2 OF 6

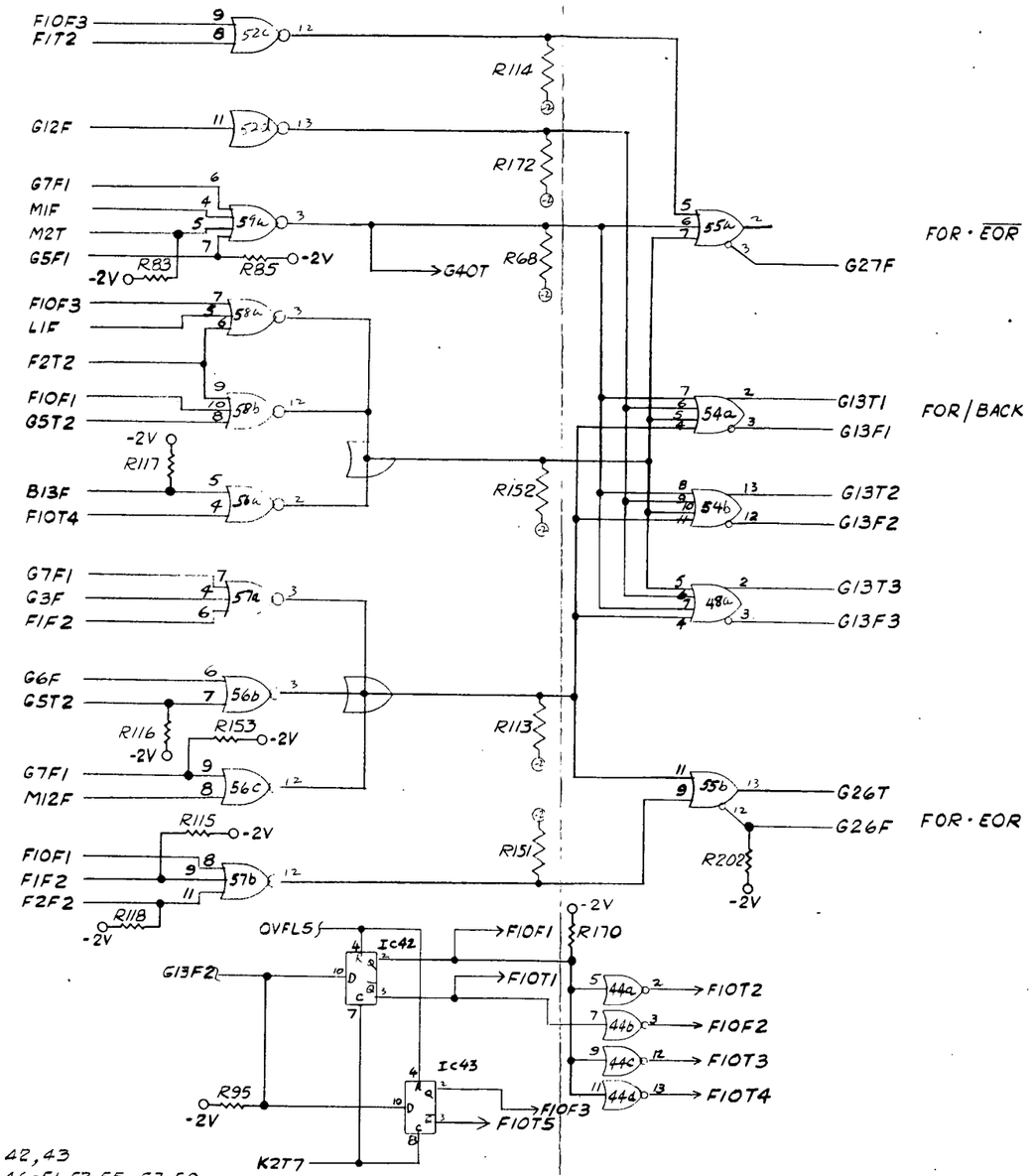
FOLDOUT FRAME 1

209

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED





MC 1670 42,43
MC 1660 46-51,53-55,57-59
MC 1662 44,45,52,56

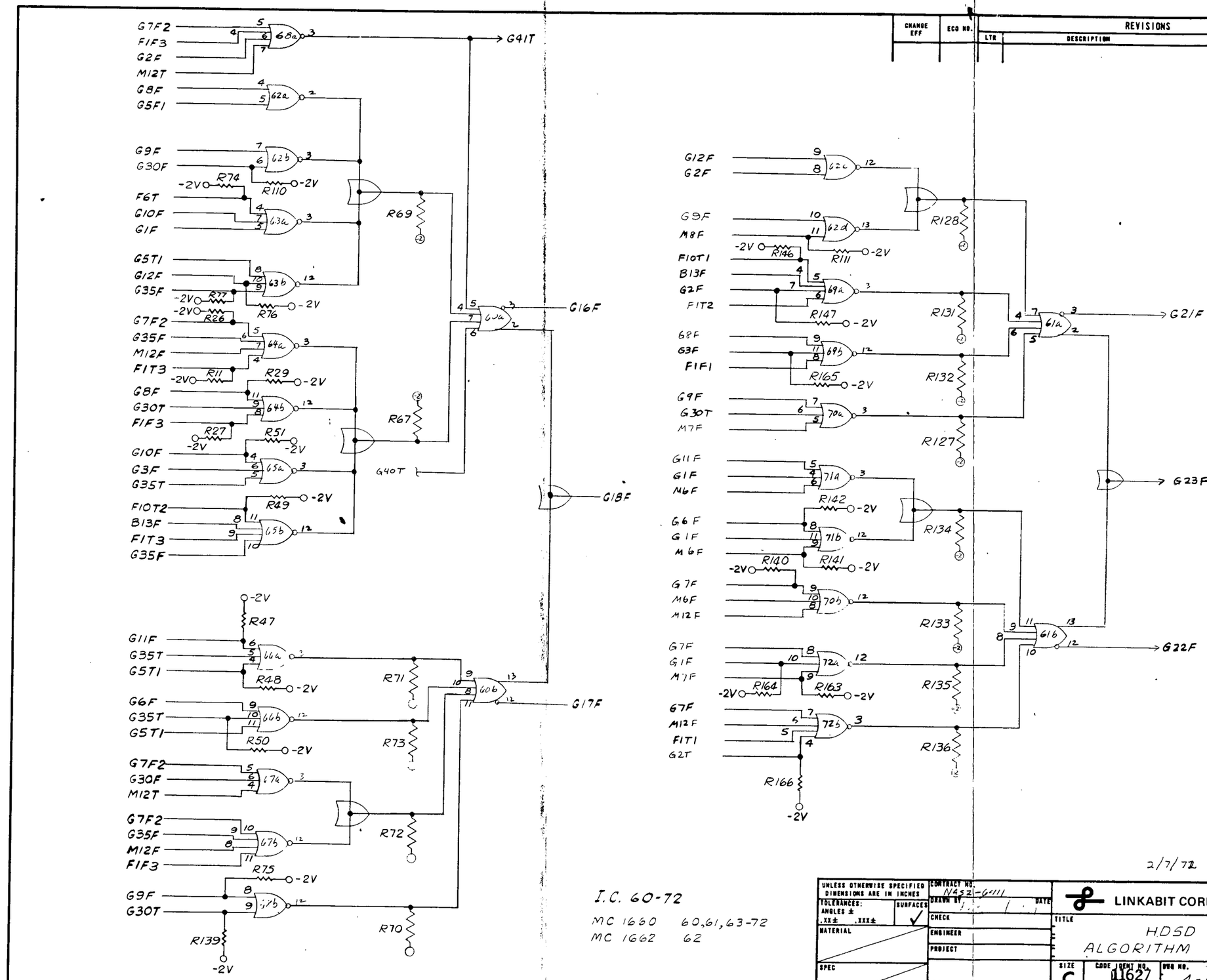
IC 42-59

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX ± .XXX ±	SURFACES ✓	DRAWN BY DATE
MATERIAL		CHECK
SPEC		ENGINEER
		PROJECT
		TITLE: HDSD ALGORITHM LOGIC
		SIZE C · CODE IDENT NO. 11627 · DWG NO. 4-000156
		SCALE — · WEIGHT — · SHEET 3 OF 6

FOLDOUT FRAME 1

210< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



I.C. 60-72

MC 1660 60,61,63-72
MC 1662 62

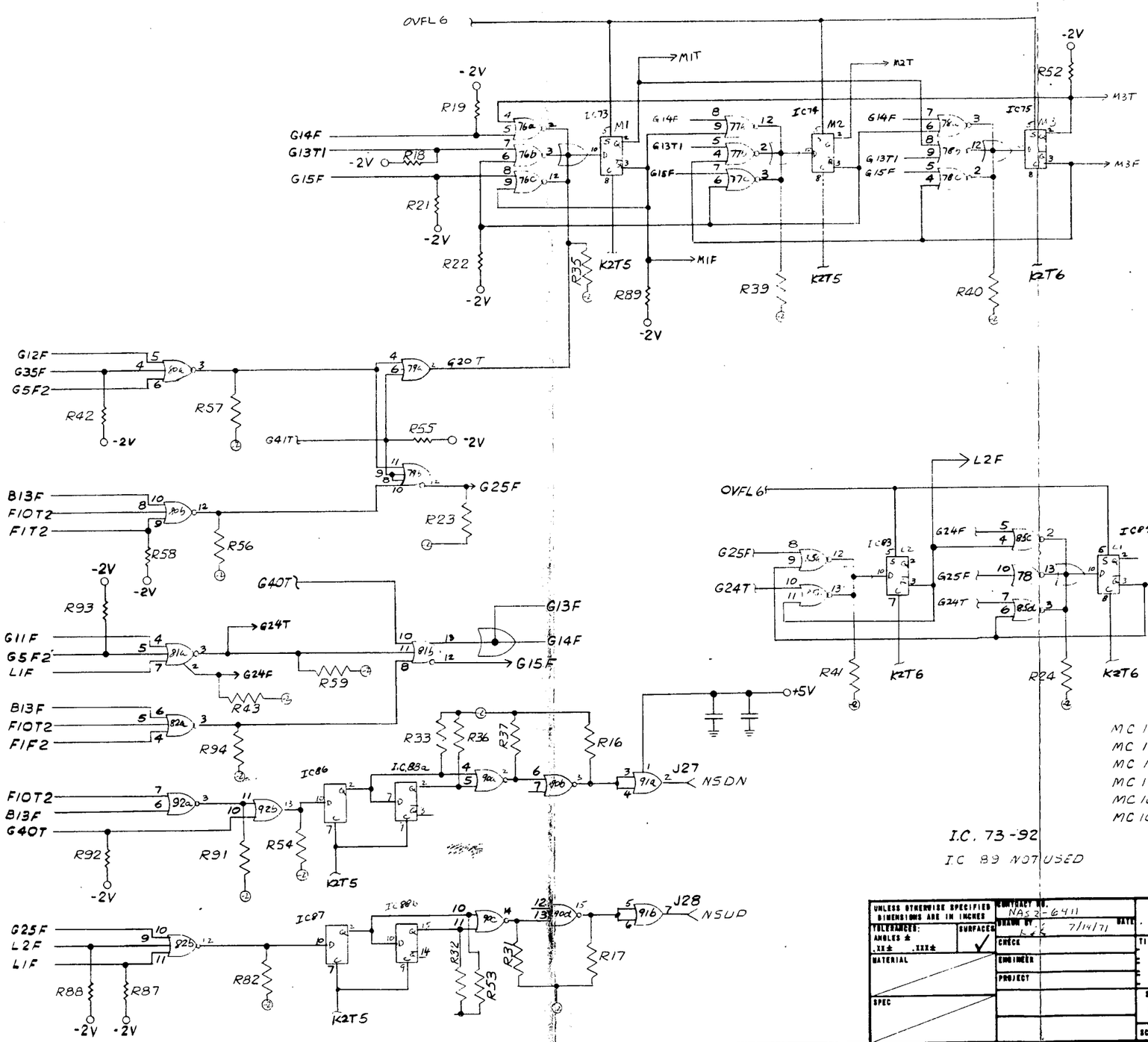
2/7/72 KB

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. N452-6111	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	TITLE: HDSD ALGORITHM LOGIC
MATERIAL	DRAWN BY DATE	
SPEC	CHECK	
	ENGINEER	
	PROJECT	
SIZE C	CODE IDENT NO. 11627	DWG NO. 4-000156
SCALE	WEIGHT	SHEET 4 OF 6

FOLDOUT FRAME 1

211< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



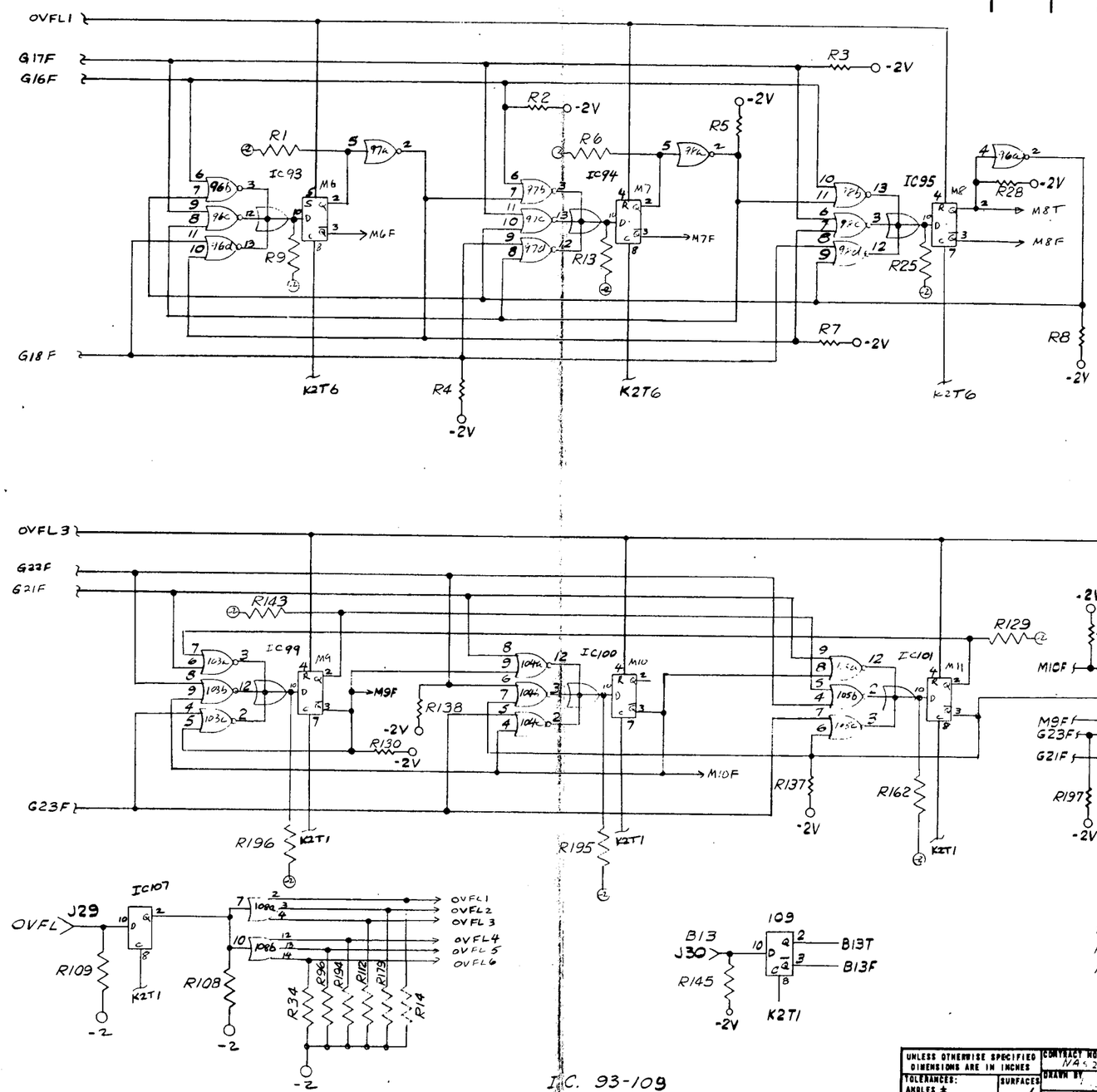
MC 1660	79-82, 92
MC 1662	76-78, 85
MC 1670	73-75, 83, 84, 86, 87
MC 10131	88
MC 10102	90
MC 1039P	91

I.C. 73-92

I.C. 89 NOT USED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX ± .XXX ±	DRAWN BY L.L. DATE 7/14/71	TITLE HDSD ALGORITHM LOGIC	
SURFACES ✓	CHECK		
MATERIAL	ENGINEER		
SPEC	PROJECT	SIZE C	CODE IDENT NO. 11627
		DWG NO. 4-000156	
		SCALE —	WEIGHT —
		SHEET 5 OF 6	

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



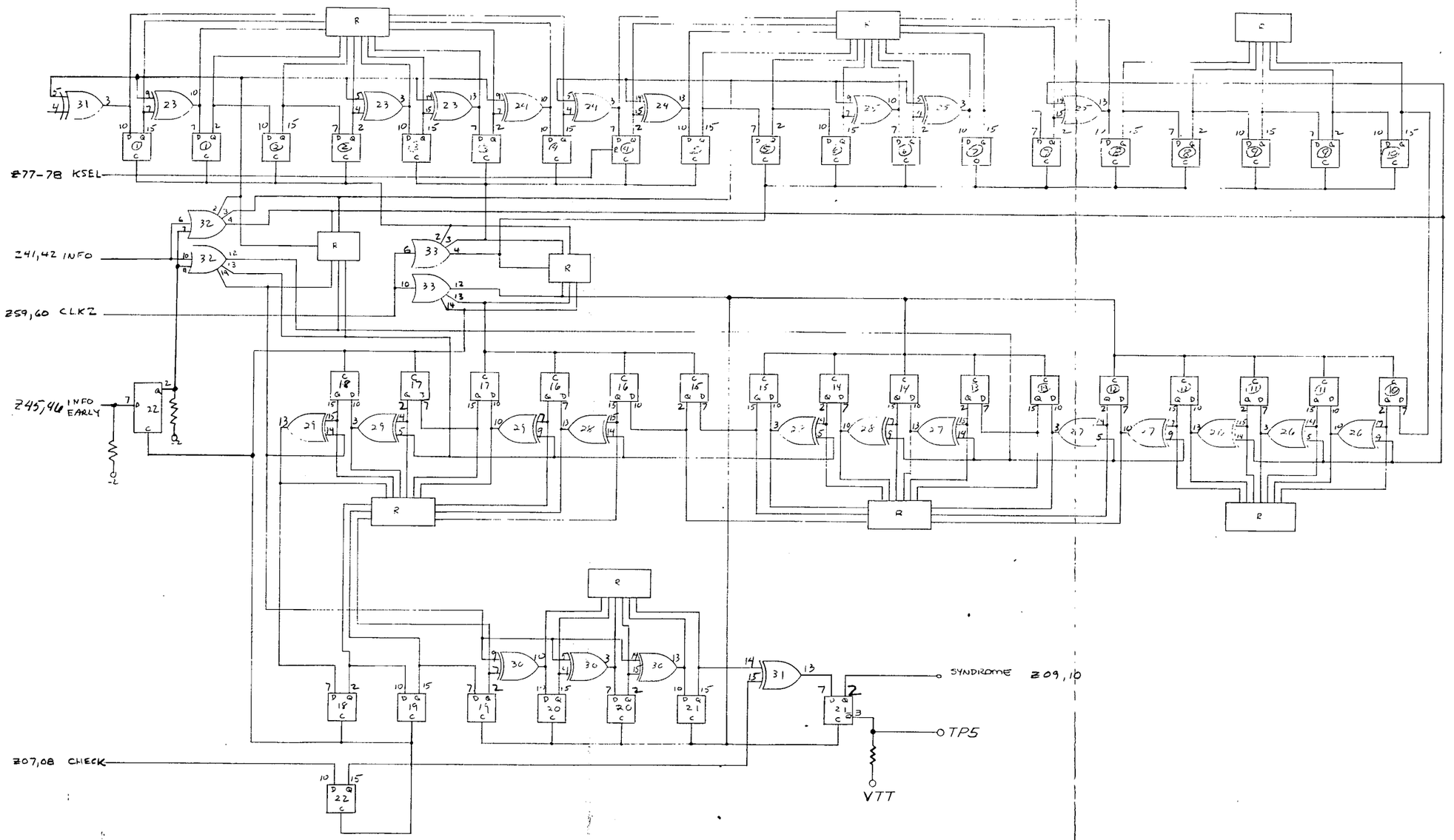
I.C.108
MC 10110

I.C. 93-109

MC 1662 96-93, 103-106
MC 1670 93-95, 99-102, 107, 109
MC 10110 108

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6111	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY	DATE
MATERIAL		CHECK	
SPEC		ENGINEER	
		PROJECT	
TITLE	HDSD ALGORITHM LOGIC		
SIZE C	CODE IDENT NO. 11627	DWG NO. 4-000156	
SCALE —	WEIGHT —	SHEET 6 OF 6	

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED



NOTE:
ALL RESISTORS ARE 899-1-R100 UNLESS OTHERWISE SPECIFIED

22	MC10131
2	MC10110
8	MC10107

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS 2-6911	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY AC 6/.. DATE	TITLE HDSD SYNDROME GENERATOR
MATERIAL		CHECK	
SPEC		ENGINEER	
		PROJECT	
		SIZE C	CODE IDENT NO. 11627
		DWG NO. 4-000157	
		SCALE —	WEIGHT — SHEET 1 OF 1

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED

CPCLK Z90 Z61

MCF CPRQF CCET MSCT JLCT SLCF LCPC TP10 ACCP PCP CPCF

270 CPUNT Z74

COMP LCYCF TP12 UNFLF SLIF SLIT IOCF RQI0

SDCLK Z86 MCF Z49 IOCLKF ICLSB

ACCP PCPF PIO ADCLF MICLK COMP LCYIO

.01μf 13K +5 150MSI IOSTF RFSL MSCT GATEB Z70 INHA Z76 GATEA Z77 INHB Z78 SLIF

CPRQF MCF CCET LCPC LCPCF SLCF

CPOVT Z72 SRCL Z60 Z75 OVCNT

ICP CPWG Z38 MCF MSAT MSCF IOWG Z22 IOCLK

MSAT MSCT SAS1 Z82 SAS2 Z83 SAS3 Z80 SAS4 Z81

MCF MARC CYHLD IOCLKF ADCLF

SLCT CPCF CPCLK WCPCA WCPCB

CYHLD PCPF MSAT MSCF PCP MICF PIO PRFT

MSAT MSCF +5 R1 R2 R4 C1 C2 C4 MCAT MCAF MCBT MCBF

MSCT +5 5K R7 680 R5 680 C2 C5 R3 680 C3 MCCF MCLKF Z58

SEL1 Z92 SEL2 Z93 SEL3 Z94 SEL4 Z95 RFSL

RCPCF Z16 LCYCP LCYIO RCPIF Z03 IOSTF MCCF

PCP CPCY PCPF PIO IOCY PIOF PRFT RFCY PCDF PLOF PRFT RFSL

MSAT MCBF RCBF Z08 680pf 470pf ADRCK

MSBT MSCF MCCLK ACCP CPRQF BUSYT

SLIT IOCF WCPIB WCPIA IOCLK SCPI Z59

MSAT MSCT

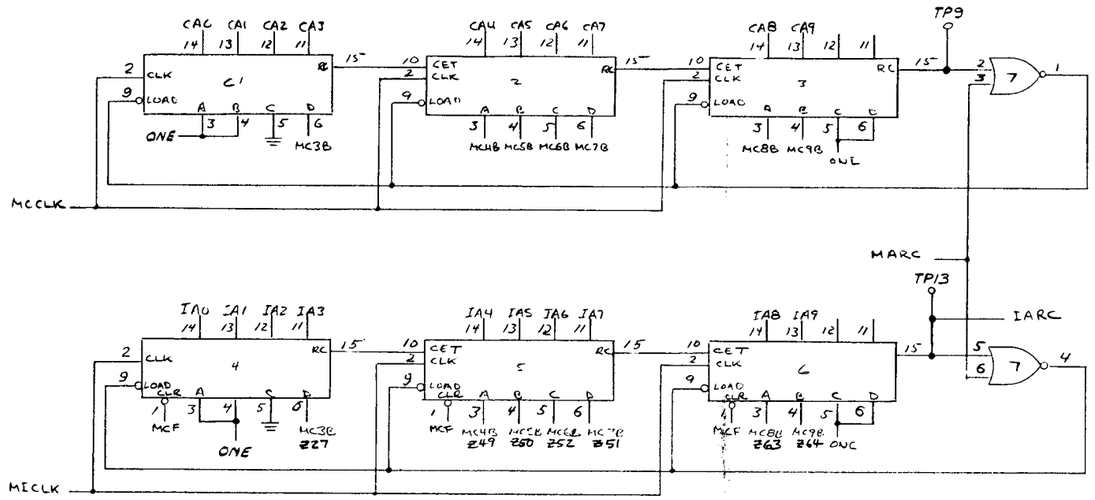
38	74H11
37	74H04
35,36	7408
34	MC9601
32	74S11
31	74S20
29,30	74S74
28	74S10
27	74H74
24,25,26	74H76
23	74H05
22	74H21
20	7432
18,33	7420
17,19	7410
15,16	7408
8,9,10,11,12,13	7400
7,14	7404
6	74HC04
4,5	74161
1,2,3,21	74C2

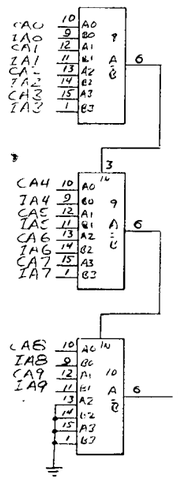
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO.	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY TC 3-1-79 DATE	TITLE	HDSD MAIN MEMORY CONTROL
SURFACES ✓	CHECK		
MATERIAL	ENGINEER		
SPEC	PROJECT	SIZE C	CODE IDENT NO. 11627
		DWG NO.	4-000158
		SCALE –	WEIGHT –
		SHEET 1	OF 3

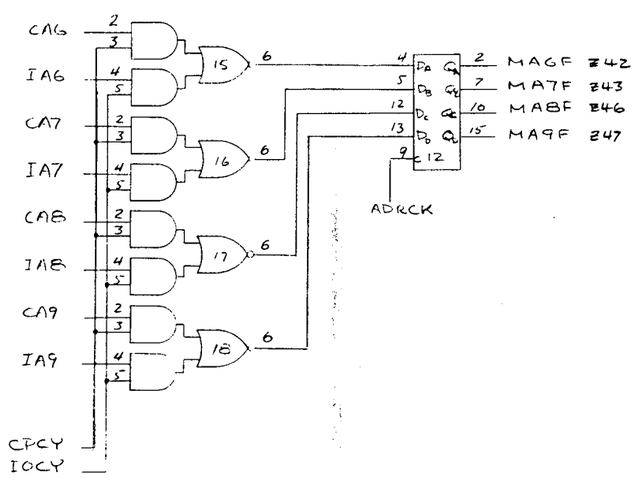
FOLDOUT FRAME

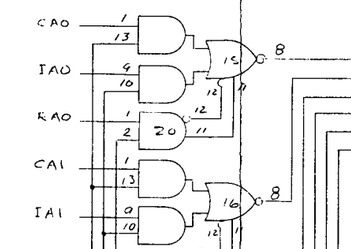
215< FOLDOUT FRAME

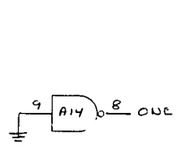
REVISIONS					
CHANGE EFF	ECO NO.	LTR	DESCRIPTION	DATE	APPROVED

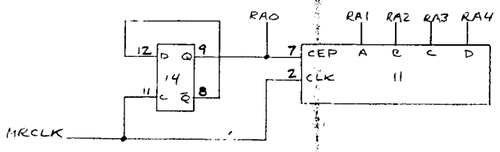












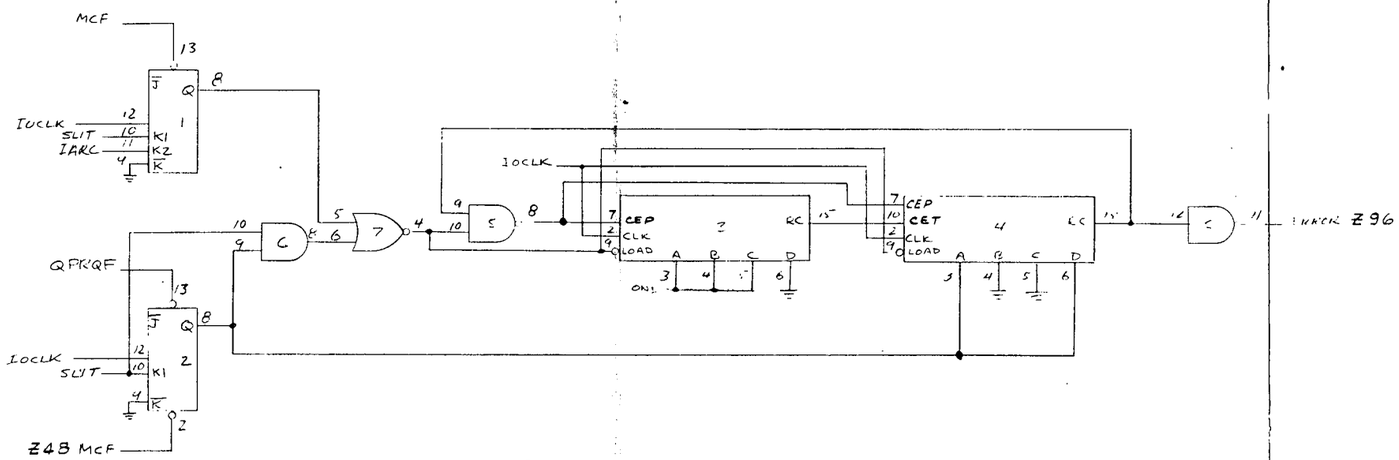
20,21,22 74H60
15,16,17,18,19 74H50
14 7474
13 74174
12 74175
8,9,10 7408
7 7402
1-6,11 74161

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO.	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY JG 6/21/82 DATE	TITLE	HDSD MAIN MEMORY CONTROL
SURFACES ✓	CHECK		
MATERIAL	ENGINEER		
	PROJECT 6000		
SPEC		SIZE C	CODE IDENT NO. [illegible] DWG NO. 4-000158
		SCALE –	WEIGHT – SHEET 2 OF 3

FOLDOUT FRAME 1

216< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED

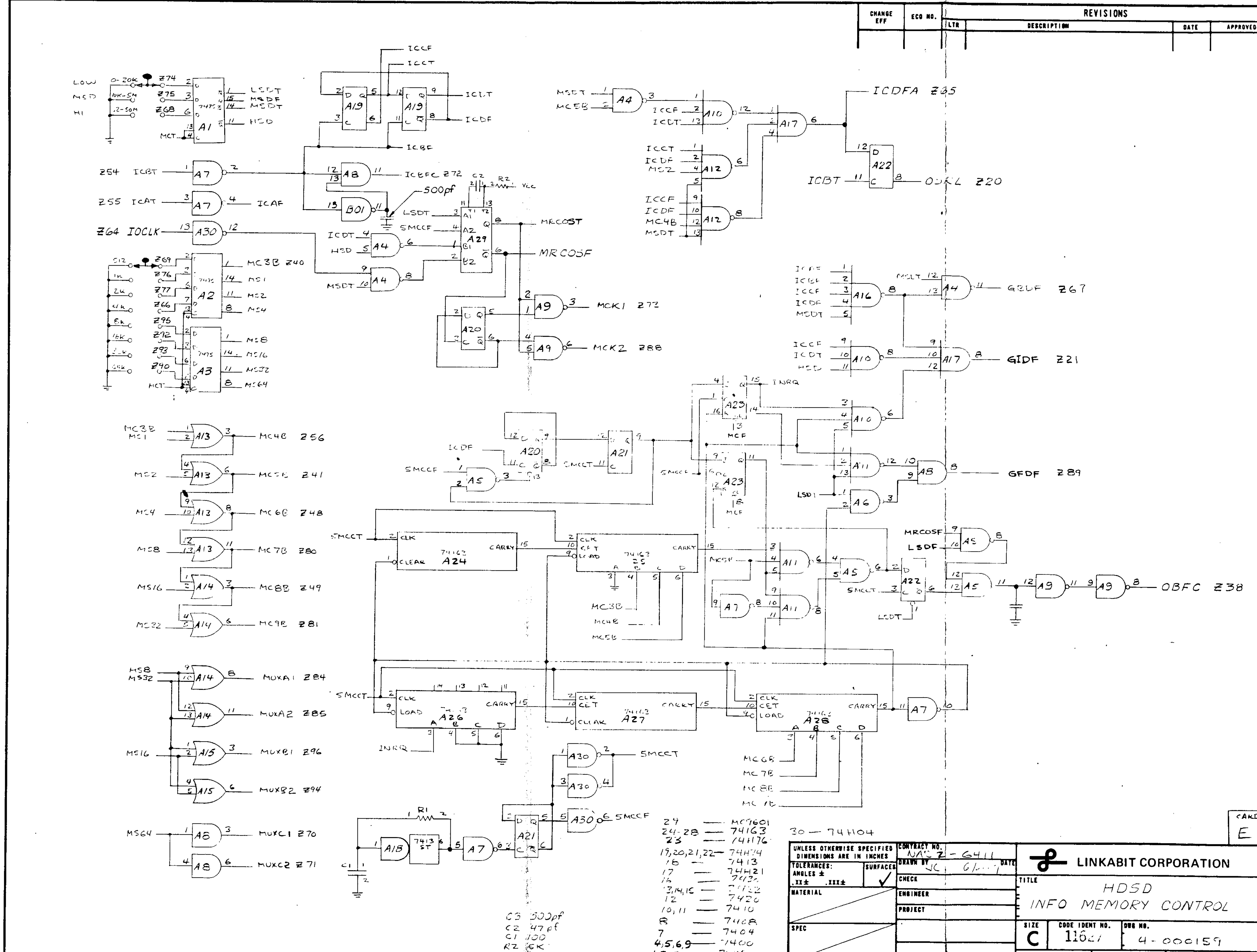


8	7400
7	7402
6	7408
5	7400
3,4	74161
1,2	7470

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO.	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY	DATE
MATERIAL		CHECK	
SPEC		ENGINEER	
		PROJECT 6600	
		TITLE: HD5D MAIN MEMORY CONTROL	
		SIZE C	CODE IDENT NO. 11627
		DWG NO. 4-000158	
		SCALE –	WEIGHT –
		SHEET 3 OF 3	

FOLDOUT FRAME 1

217< FOLDOUT FRAME 2



CHANGE EFF	ECO NO.	LTR	DESCRIPTION	DATE	APPROVED

24 — MC7601
24-28 — 74163
23 — 74H76
19,20,21,22 — 74H74
18 — 7413
17 — 74H21
13 — 7413
3,14,15 — 7432
12 — 7420
10,11 — 7410
8 — 7408
7 — 7404
4,5,6,9 — 7400
1,2,3 — 7475

30 — 74H04

C3 500pf
C2 47pf
C1 .100
R2 5K
R1 330

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± .XX± .XXX±
SURFACES ✓
MATERIAL
SPEC
CONTRACT NO. NAS 2-6411
DRAWN BY JC
CHECK
ENGINEER
PROJECT

LINKABIT CORPORATION

TITLE HDSD INFO MEMORY CONTROL

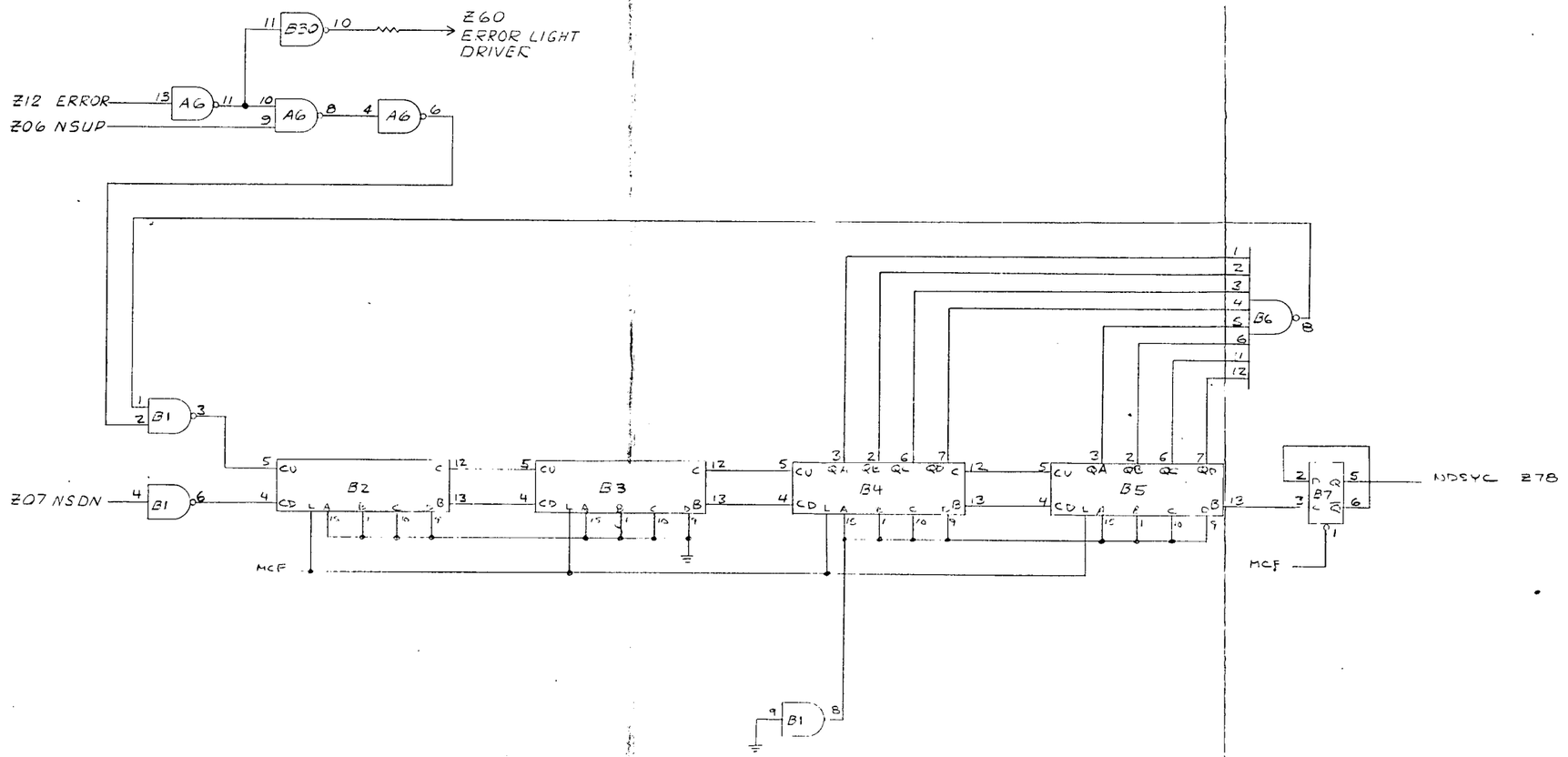
SIZE C | CODE IDENT NO. 11621 | DWG NO. 4-000159
SCALE | WEIGHT | SHEET 1 OF 2

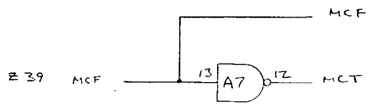
CARD E

FOLDOUT FRAME

218< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED





7 — 7474
6 — 7430
2,3,4,5 — 74193
1 — 746[illegible]

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. 6000	LINKABIT CORPORATION	CARD E
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY JC DATE	TITLE HDSD INFO MEMORY CONTROL	
MATERIAL	CHECK		
SPEC	ENGINEER		
	PROJECT	SIZE C CODE IDENT NO. 11627 DWG NO. A-[illegible]159	
		SCALE – WEIGHT – SHEET 2 OF –	

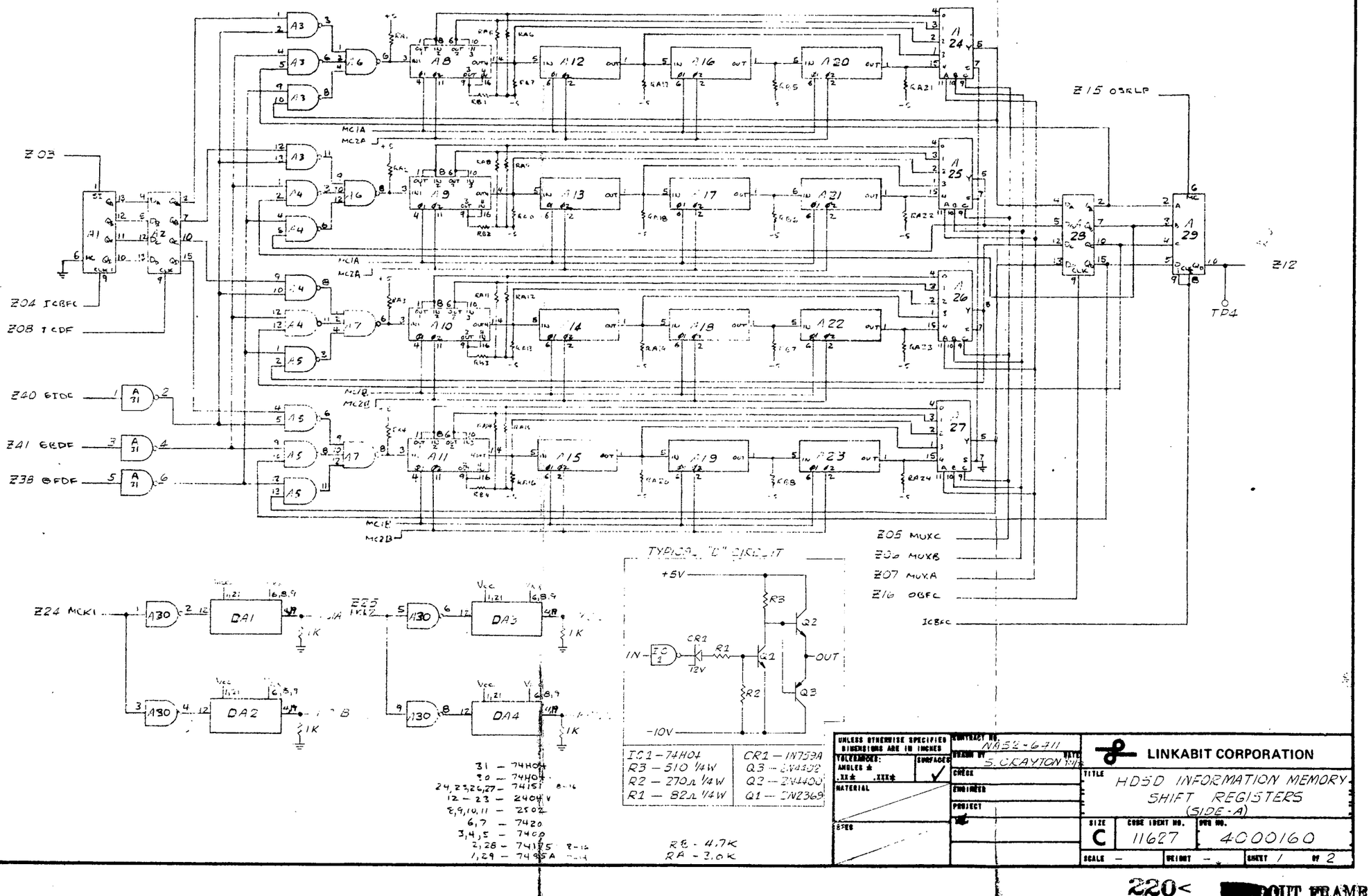
FOLDOUT FRAME 1

219< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED

SIGNAL

CARD LOCATION		Z03	Z12
	C	IB0	IDB0
	D	IB2	IDB2



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS2-6411	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY S. CRAYTON DATE	TITLE HDSD INFORMATION MEMORY SHIFT REGISTERS (SIDE-A)
SURFACES ✓	CHECK	
MATERIAL	ENGINEER	
FINISH	PROJECT	SIZE C · CODE IDENT NO. 11627 · DWG NO. 4000160
		SCALE — · WEIGHT — · SHEET 1 OF 2

OLDOUT FRAME 1

220<

OLDOUT FRAME 2

SIGNAL		Z62	Z83
CARD LOCATION	C	IB1	IDB1
	D	IA3	IDB3

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED

Z62

Z63 IOBFC

Z80 IODF

EIOC

ERDF

EFDF

Z85 OSRLP

Z83

TP10

Z60 MUXC

Z61 MUXB

Z58 MUXA

Z86 OBFC

IOBCC

MCIA

MCIB

MCIK

MCKI

DB1

DB2

DB3

DB4

1K

31 – 74H08
30 – 74H00
24,23,26,27 – 7415 8-16
12 – 23 – 2405N
8,9,10,11 – 2502
6,7 – 7423
3,4,5 – 7402
2,28 – 7417 8-16
1,29 – 7495A 7-14

RB – 4.7K
RA – 3.0K

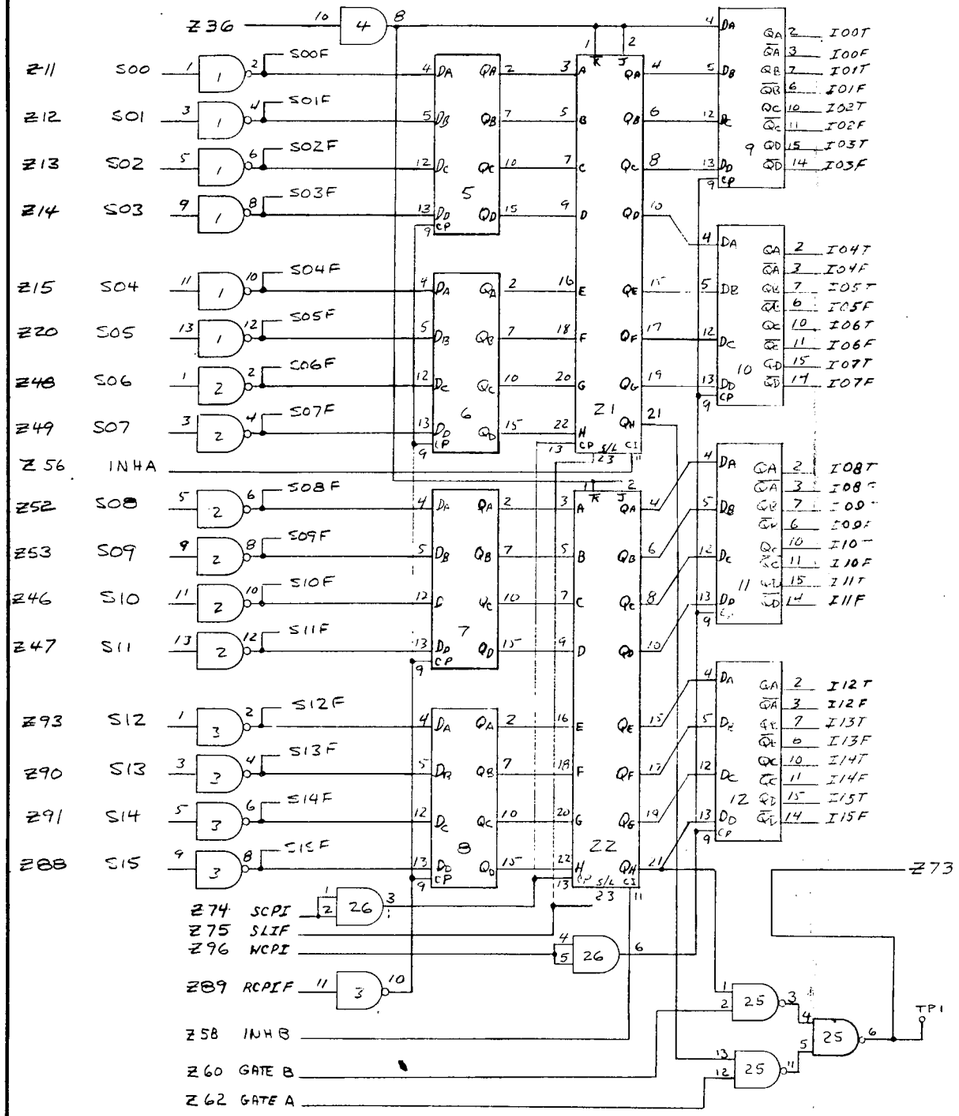
SEE SHT 1 FOR "D" CIRCUIT CONFIG

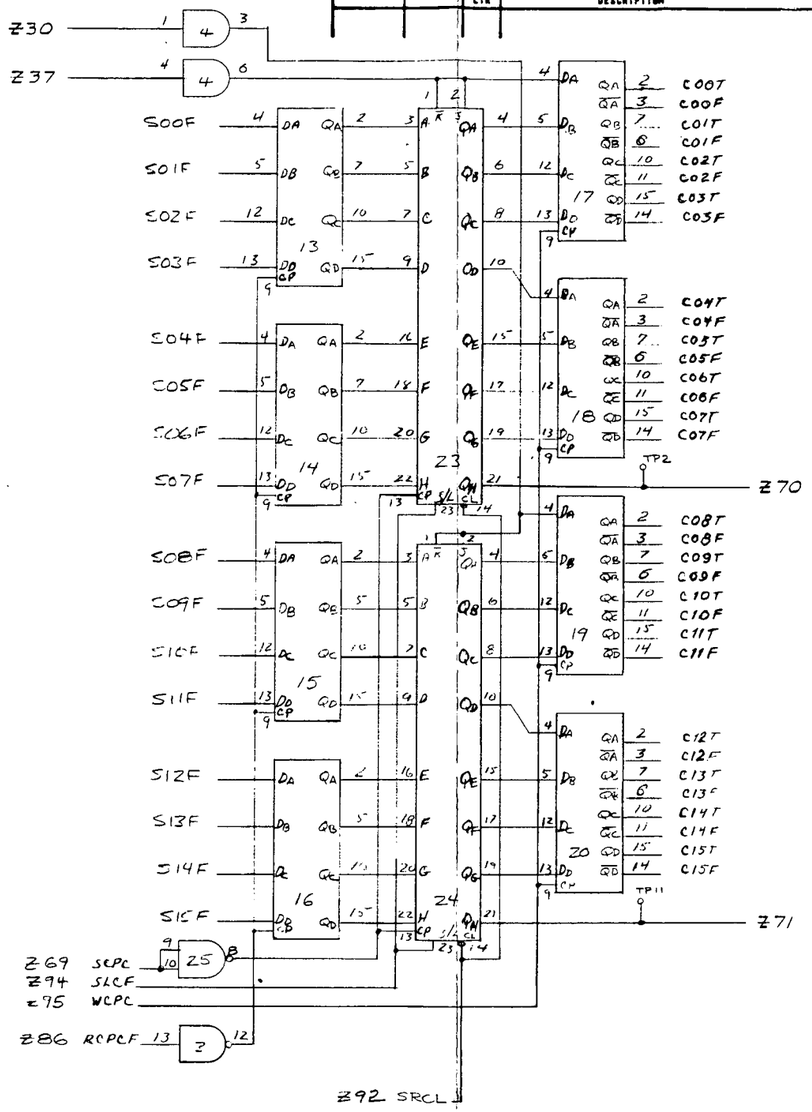
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	COMPILED BY	LINKABIT CORPORATION
TOLERANCES: ANGLES ± .XX ± .XXX	DRAWN W. SCRAYTON 7/23/75	TITLE HDSD INFORMATION MEMORY SHIFT REGISTERS (SIDE B)
SURFACES ✓	CHECK	
MATERIAL	ENGINEER	
SPEC	PROJECT	SIZE C · CODE IDENT NO. 11627 · DWG NO. 4000160
		SCALE · WEIGHT · SHEET 2 OF 2

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS					
CHANGE EFF	ECO NO.	LTR	DESCRIPTION	DATE	APPROVED





CARD LOCATIONS	Z36	Z30	Z37	Z73	Z70	Z71
F	SB0	B3ITC	B7ITC	SDB0	B7ØTC	B3ØTC
H	SB1	B2ITC	B6ITC	SDB1	B6ØTC	B2ØTC
K	SB2	B1ITC	B5ITC	SDB2	B5ØTC	B1ØTC
M	SB3	B0ITC	B4ITC	SDB3	B4ØTC	B0ØTC

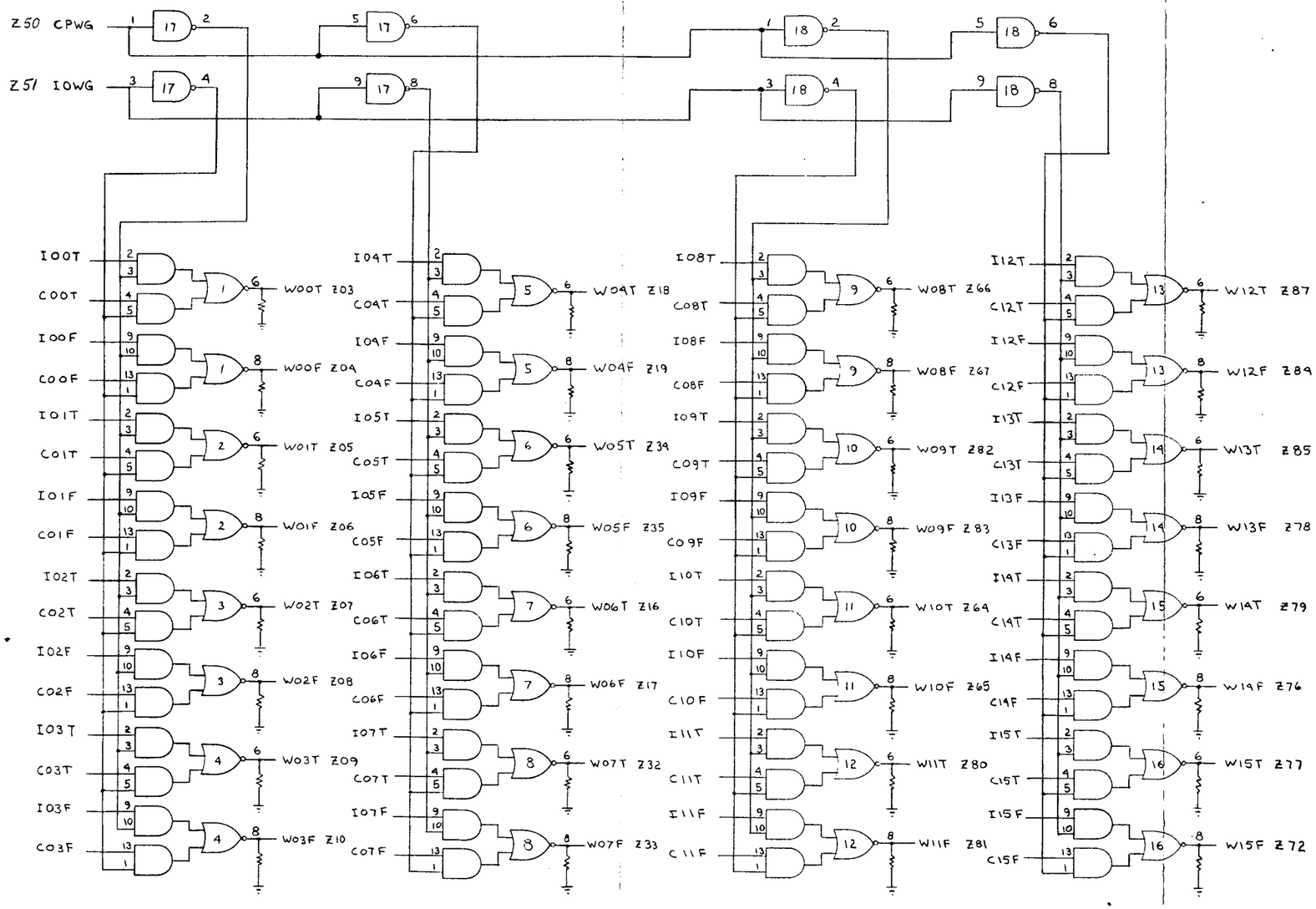
25	74H00
21-24	74199
5-20	74175
4,26	7408
1,2,3	74H04

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. 6000	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY JC DATE	TITLE	MAIN MEMORY BUFFER
MATERIAL	CHECK		
SPEC	ENGINEER		
	PROJECT	SIZE C	CODE IDENT NO. 11627
		SCALE —	WEIGHT —
		SHEET 1 OF 2	DWG NO. 4-000164

FOLDOUT FRAME 1

222< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED



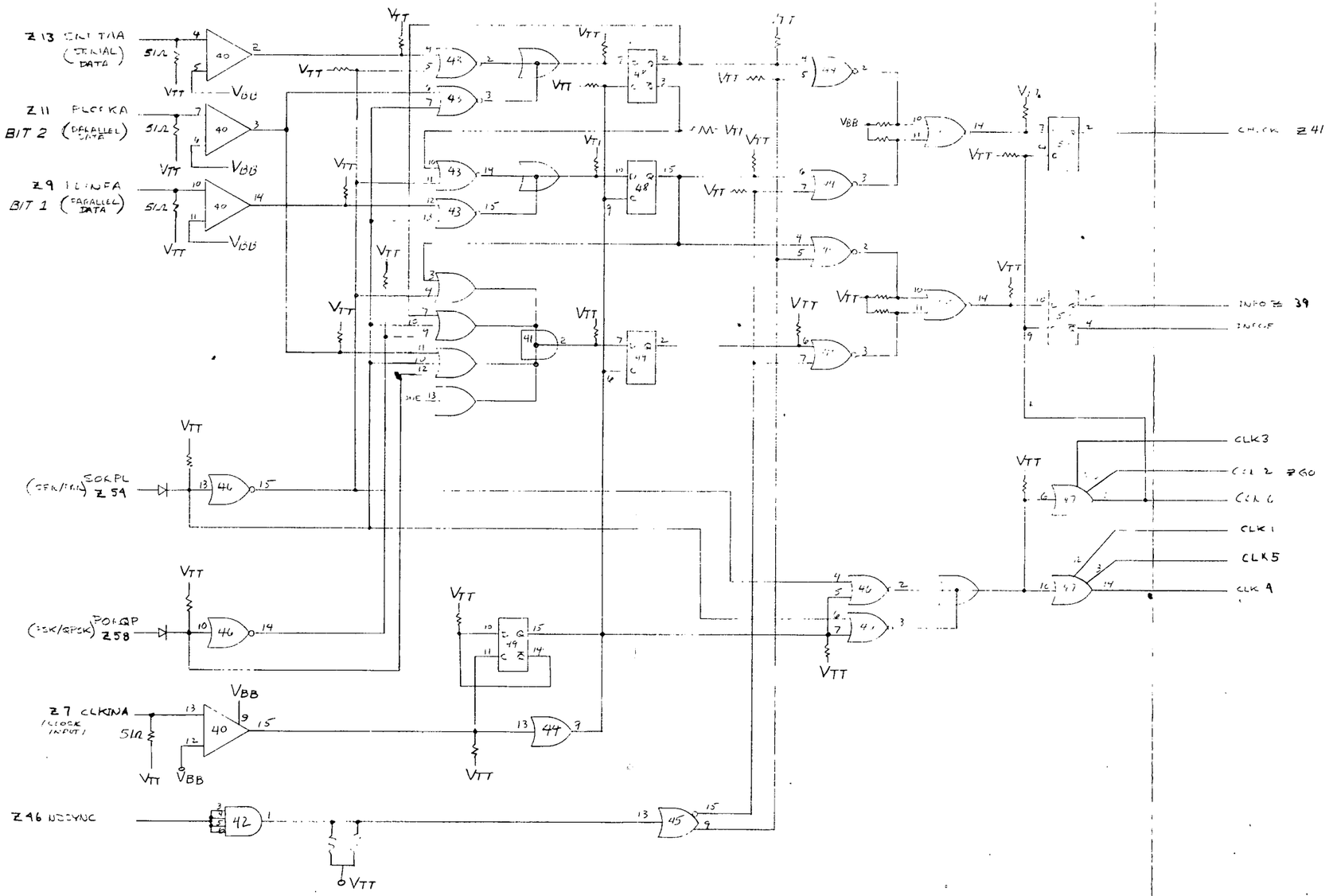
ALL RESISTORS 1K (01-1023)
17,18 7404
1-16 7451

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. 6000	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	DRAWN BY J. C DATE	TITLE MAIN MEMORY BUFFER	
SURFACES ✓	CHECK		
MATERIAL	ENGINEER		
	PROJECT	SIZE C	CODE IDENT NO. 11627
SPEC		DWG NO. 4-000164	
		SCALE —	WEIGHT —
		SHEET 2 OF 2	

FOLDOUT FRAME 1

FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS			
		LTR	DESCRIPTION	DATE	APPROVED



48-50 MC 10131-16
47 MC 10110-16
43-46 MC 10102 - 16
42 MC 1017 - 14
41 MC 10119 - 16
40 MC10115 - 16

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS 5-6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX±	SURFACES ✓	DRAWN BY JC DATE	TITLE 4050 INPUT/OUTPUT
MATERIAL		CHECK	
SPEC		ENGINEER	SIZE C / CODE IDENT NO. 11617 / DWG NO. 4-000172
		PROJECT	SCALE — / WEIGHT / SHEET 1 OF 2

FOLDOUT FRAME 1

224< FOLDOUT FRAME 2

CHANGE EFF	ECO NO.	REVISIONS LTR	DESCRIPTION	DATE	APPROVED

Z19 SYNTHCME

Z 20 SDCK

Z 21 SDC1

Z 62 SDC1

Z 17 SDC2

Z 80 SDC2

Z 18 SDC3

Z 81 SDR3

INFOF

IBO Z32

IB1 Z40

IB2 Z30

IB3 Z31

IDCLK Z69

IDCLK Z56

Z 48 MSDS

SDCLK Z55

Z 87 IDCO

Z89 IDB1

Z91 IDB2

Z85 IDB3

Z99 ERROR

Z72

CLOCK1 Z 90

CLOCK2 Z 93 NOT USED

ERR1 Z 94

ERR2 Z 57 NOT USED

DATA1 Z 59

DATA2 Z 71 NOT USED

TP13

TP100

NC 24 ONE

34-37	MC 10131	-16
23-	MC 10109	-
29-33	MC 1017	- 4
26,27,28	MC 1039	- 6
25	MC 10107	-
24	MC 10111	-16
19-22	MC 10102	-16
15-18	MC 10110	-16
1-14	MC 10131	-16

MC 1017 +E PIN 8
MC 1039 +E PIN 1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO. NAS 2 - 6411	LINKABIT CORPORATION	
TOLERANCES: ANGLES ± .XX± .XXX± SURFACES ✓	DRAWN BY NC DATE	TITLE HDSD INPUT/OUTPUT	
MATERIAL	CHECK		
SPEC	ENGINEER		
	PROJECT	SIZE C	CODE IDENT NO. 11627
		DWG NO. 4-000172	
		SCALE —	WEIGHT —
		SHEET 2 OF 2	

OUTPUT FRAME 1

OUTPUT FRAME 2